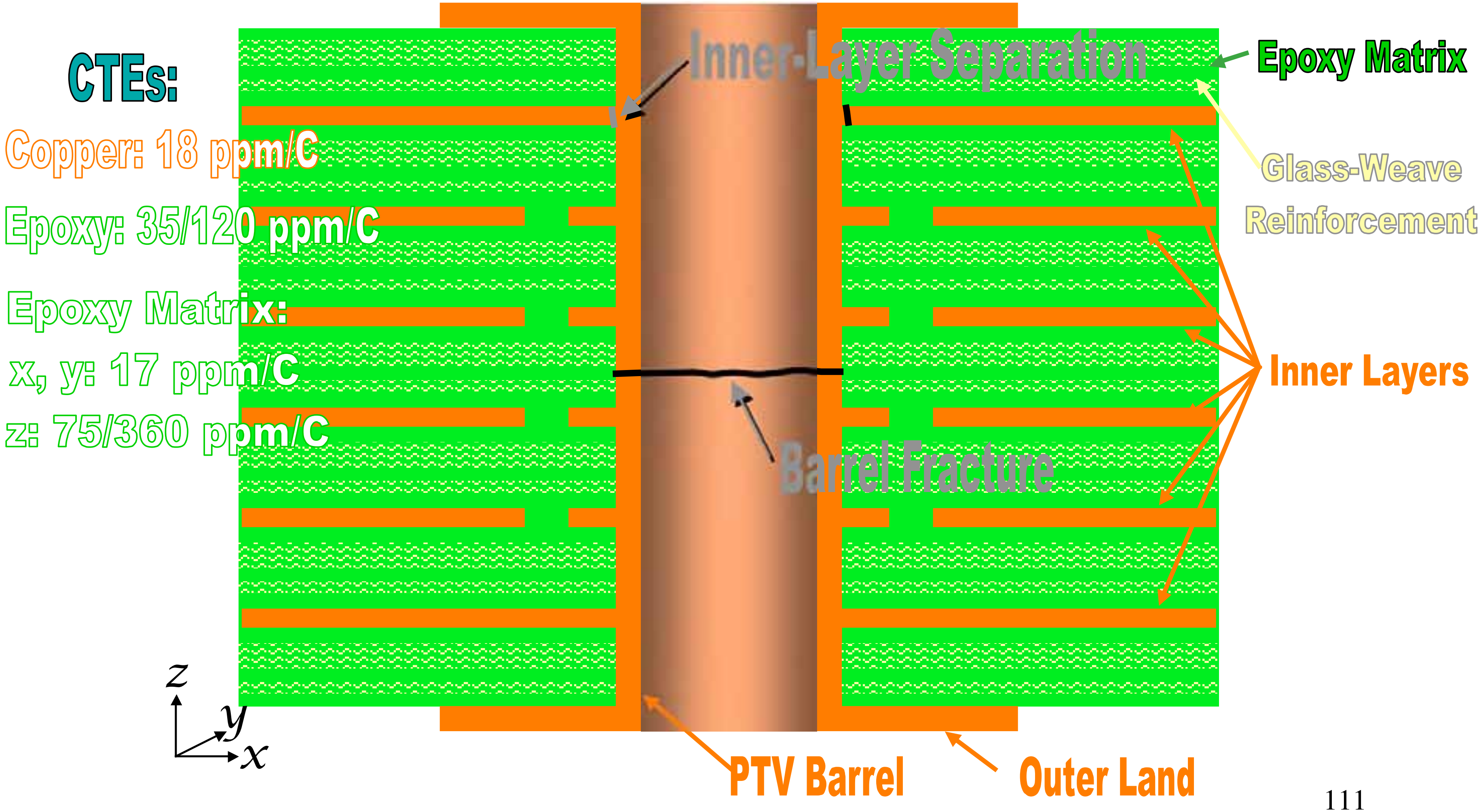
Outline

- Reliability & Threat to Reliability
- Lead-Free Solder Issues
- Solder Joints
  - Failure Modes & Load Drivers
  - Solder Creep-Fatigue Behavior & Modeling
- Printed Wiring Boards
  - Failure Modes & Load Drivers
- Components
  - Failure Modes & Load Drivers
- Reliability Assurance Tests
  - Solder Joints
  - PCBs
  - Components

PTH/PTV Interconnect Structure



Printed Circuit Boards : Load Drivers (1)

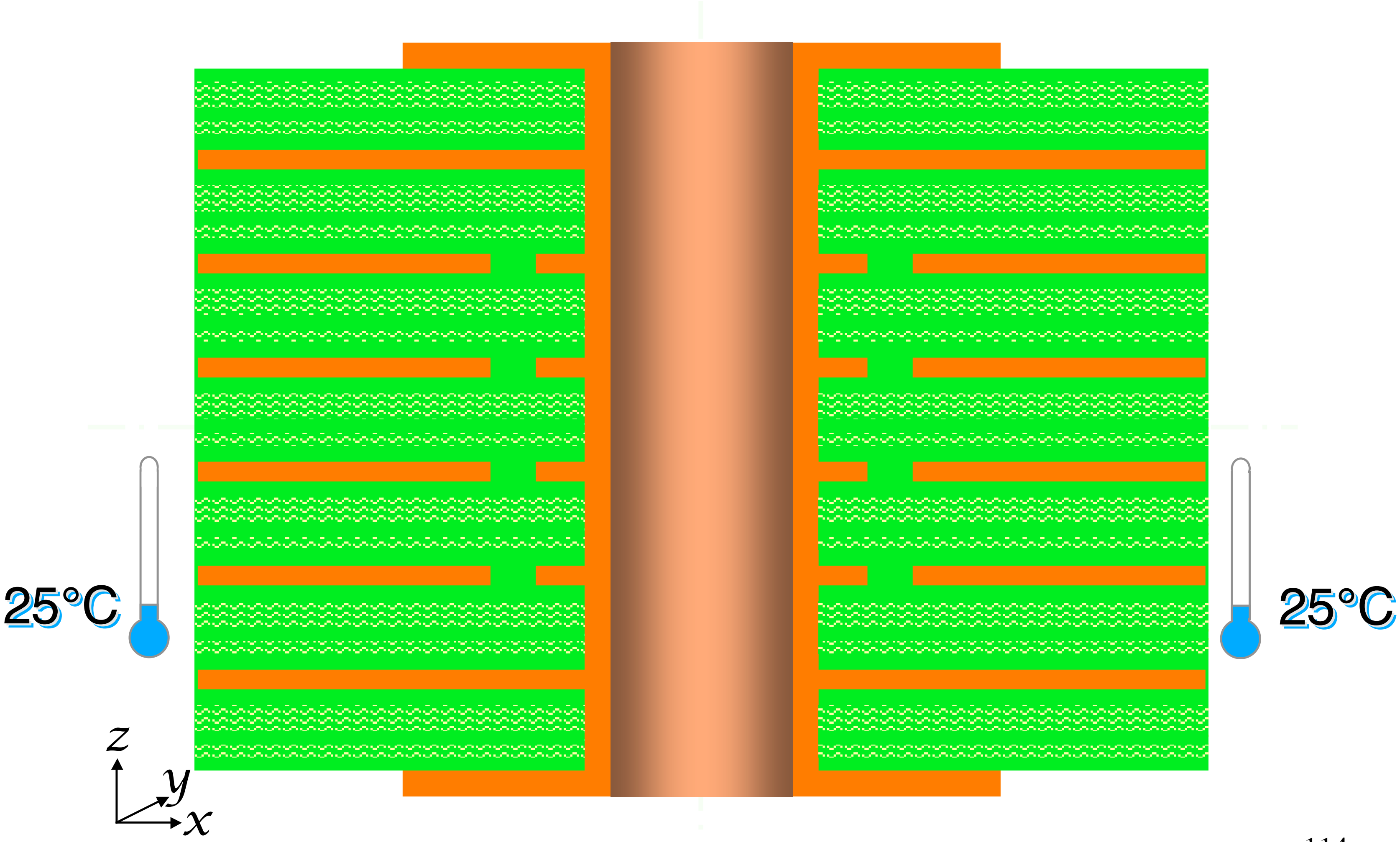
- The primary load driver is the thermal expansion mismatch between the PWB resin and the PTH/PTV copper barrel
  - The resin is prevented from expanding in x/y by the PWB glass reinforcement. Thus, the resin expansion occurs in the z-direction at almost 3x the linear expansion of just resin.
  - ➢ Thus, the PTH/PTV barrel is stressed in tension in z.
  - The resin expansion stresses the barrel in compression in x/y, which put the inner-layer connects in tension.
  - ➢ Thus, the inner-layer connects are in tension radially in x,y.

Soldering Processes

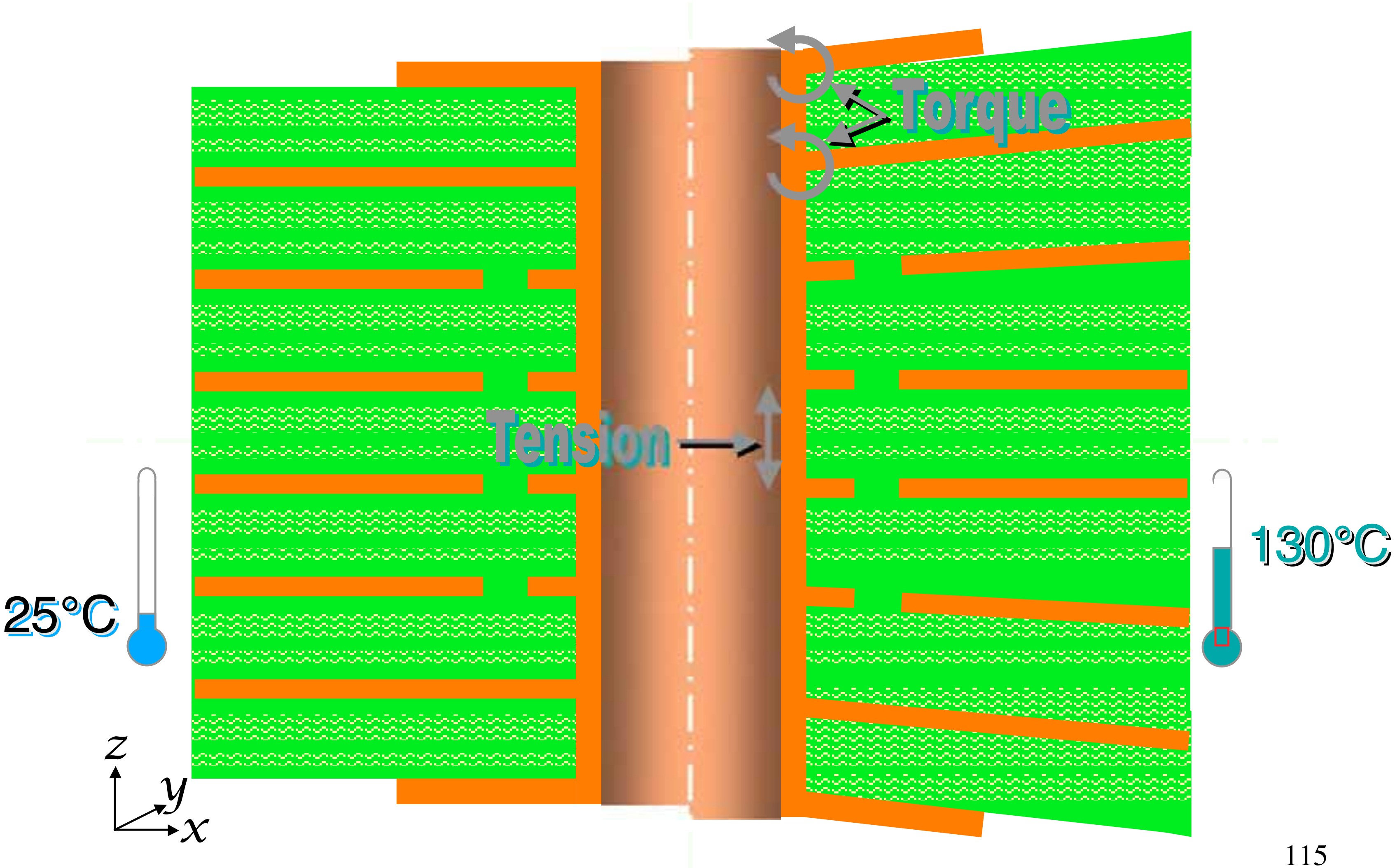
- Hot-Air Solder Leveling (HASL) —250//280°C
- Infrared (IR) Reflow —225//265°C
- Forced Convection Reflow —220//260°C
- Wave Soldering —240//260°C
- Hand Soldering —≤290//310°C

Note: These temperatures for SnPb-soldering and SAC-soldering.

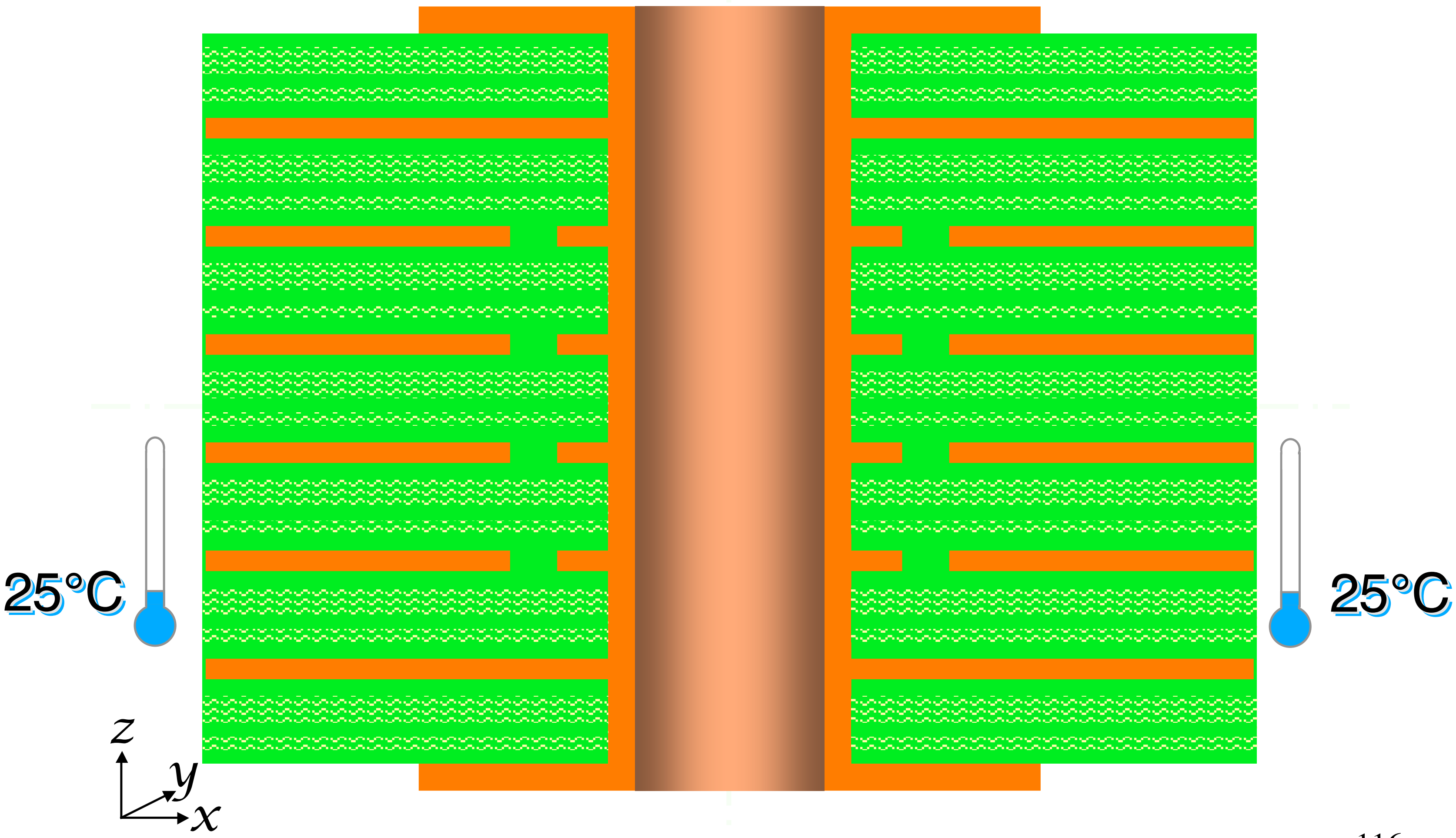
PTH/PTV Interconnect Structure



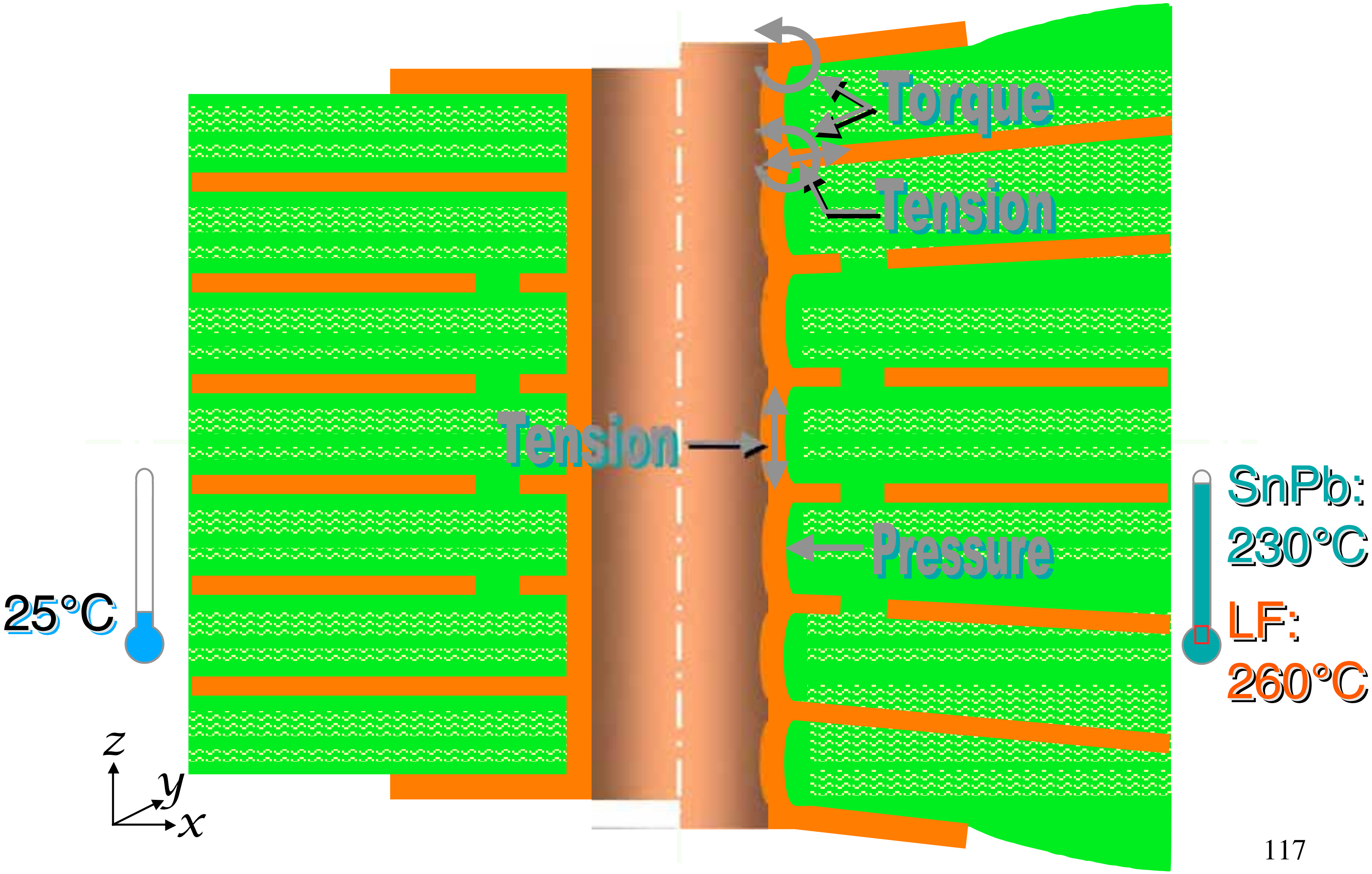
PTH/PTV Interconnect Structure



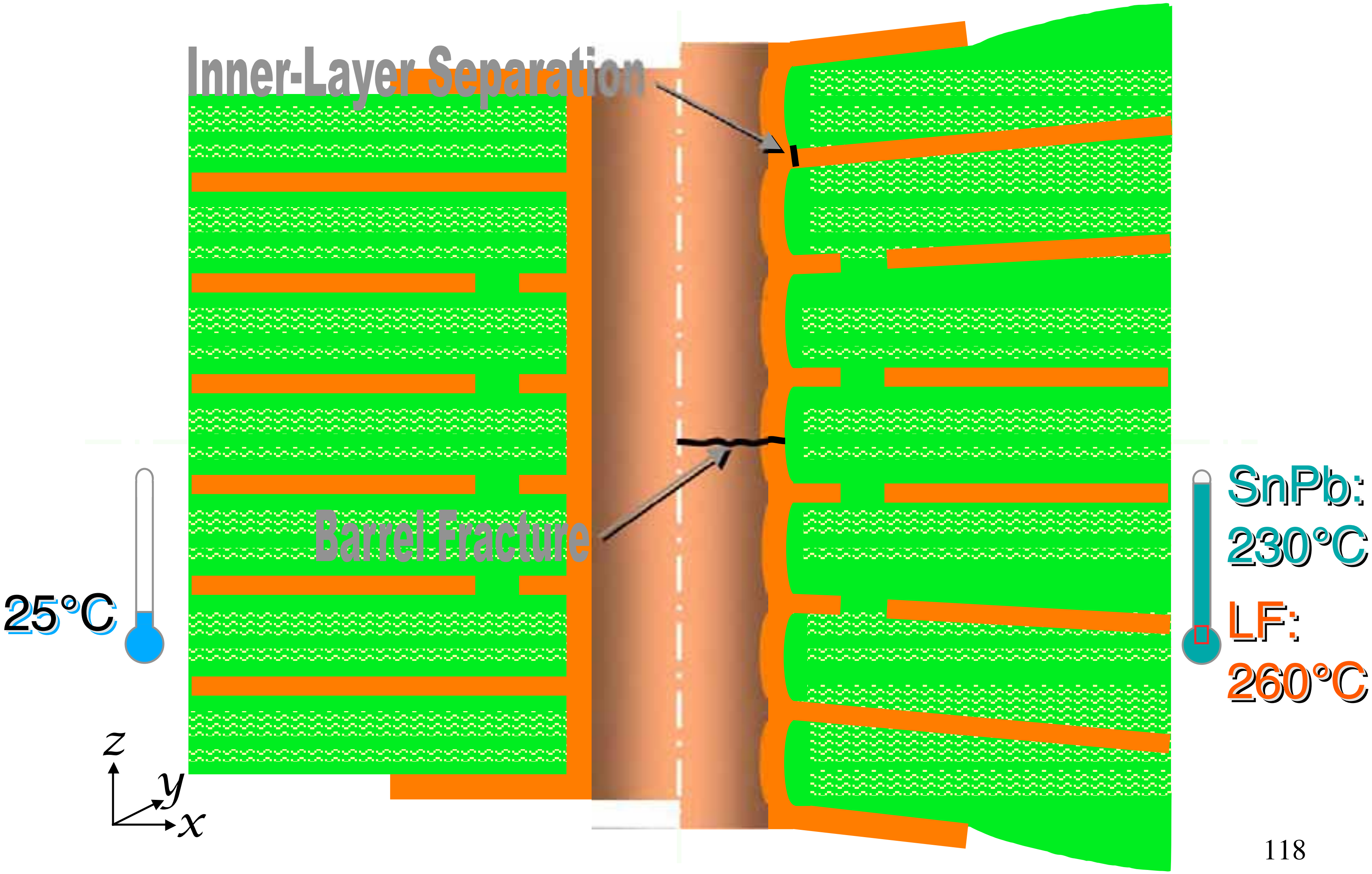
PTH/PTV Interconnect Structure



PTH/PTV Interconnect Structure

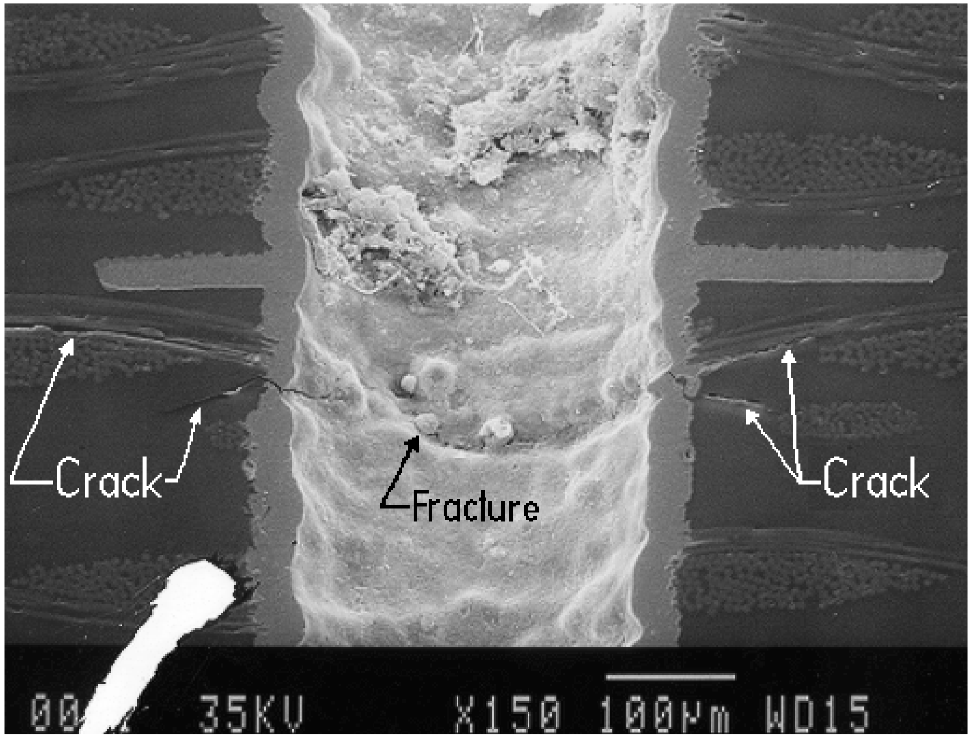


PTH/PTV Interconnect Structure



Plated-Through Via [PTV] Barrel Crack

<u>Note:</u> Cu plating along glass bundle cracks, resulting in locally thinner plating of PTV wall; these stress concentrations cause the barrel fracture



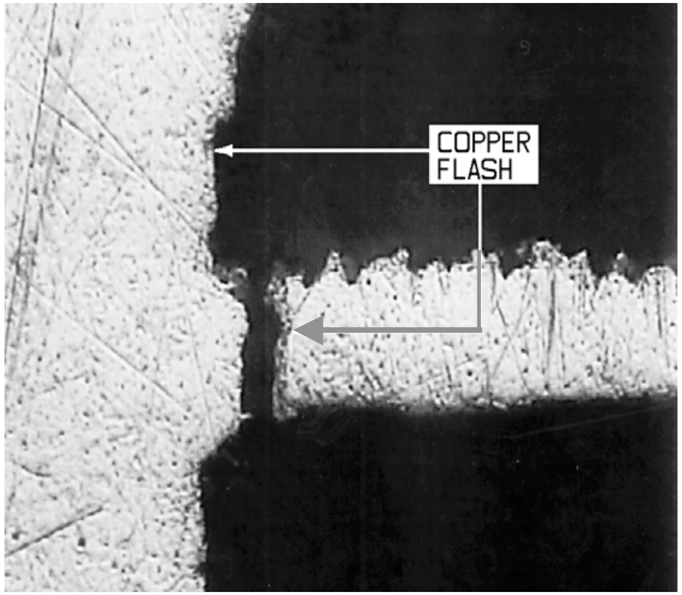
Via Inner-Layer Separation

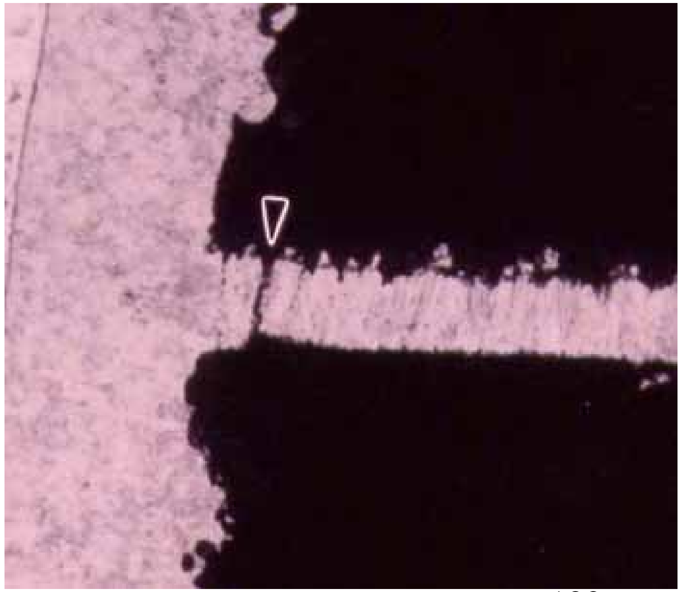
Inner-layer separation (ILS) between the PTV barrel and inner-layer. Three possible failure modes:

(1) electrolytic copper plating/electroless copper flash (top);

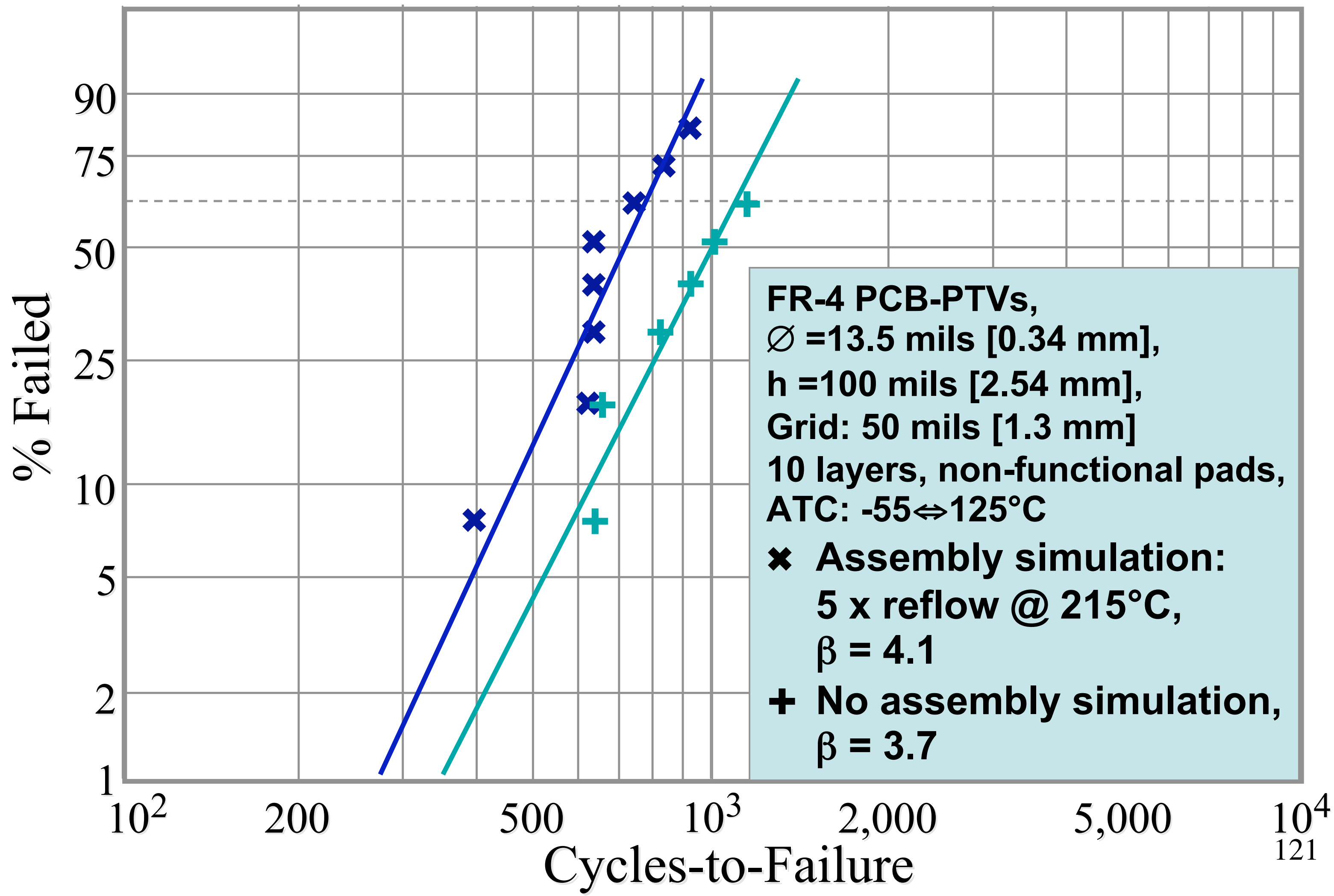
(2) electroless copper flash/copper foil;

(3) copper foil (bottom).





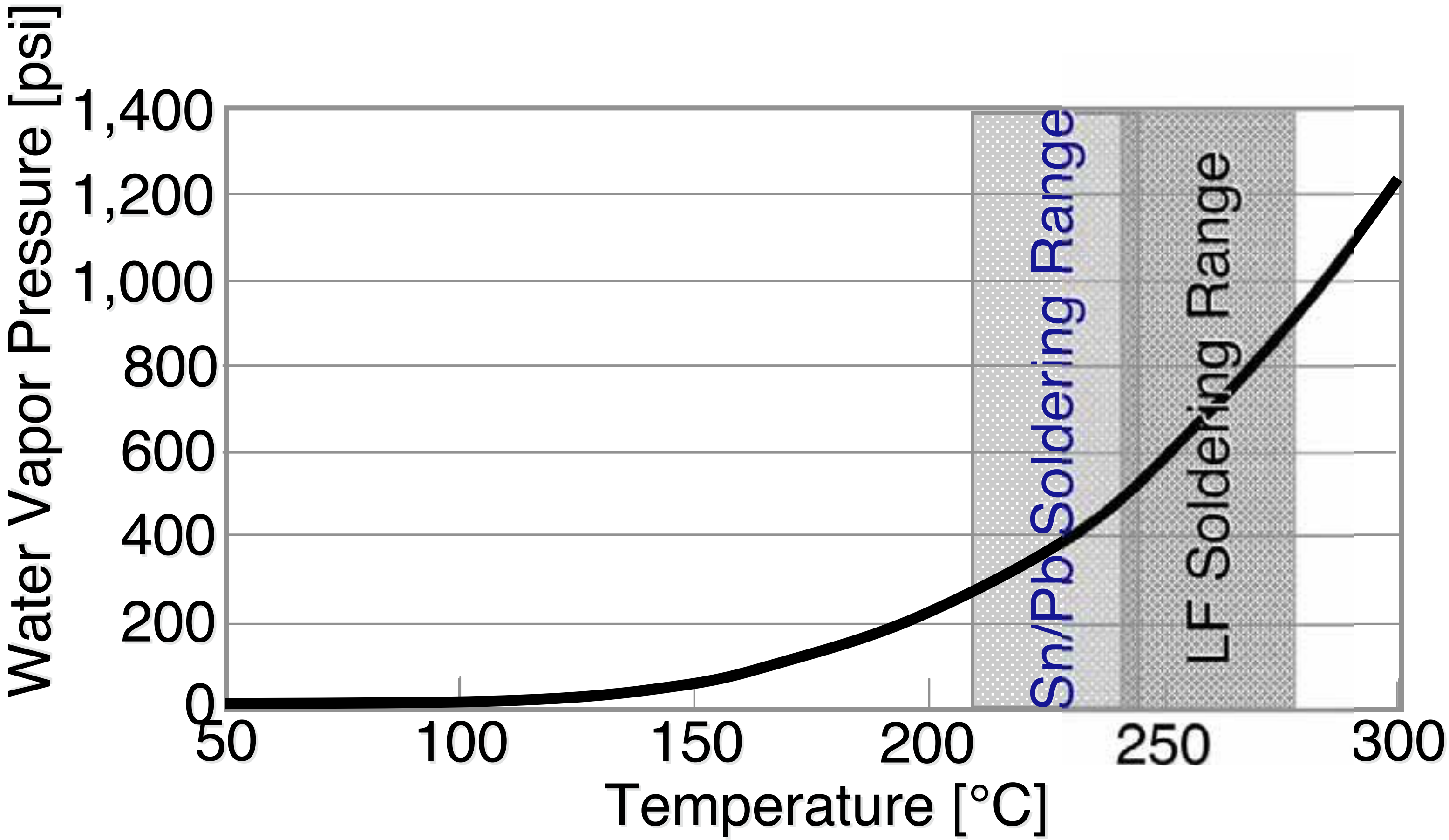
Weibull Distribution for PTV Coupons



Printed Circuit Boards : Load Drivers (2)

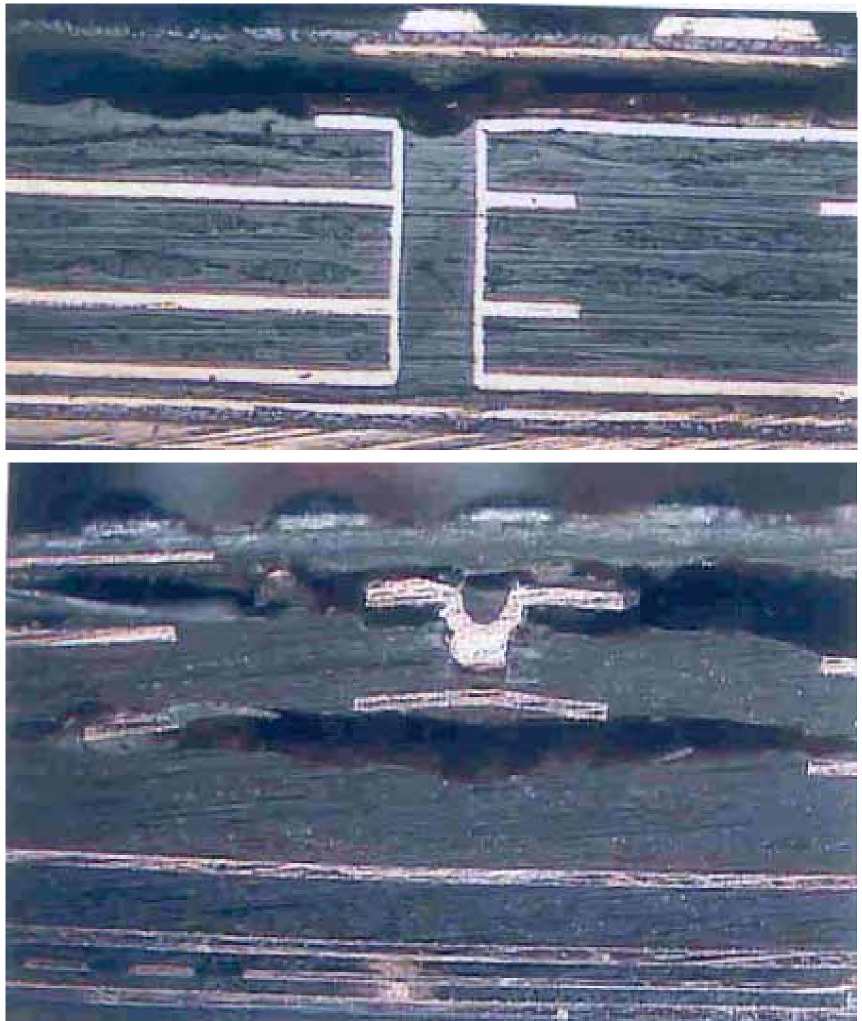
- Another important load driver is absorbed moisture within the PCB
  - PCB resins absorb moisture; this moisture can be removed prior to soldering processes by a moisture removal baking step.
  - The higher soldering temperatures for LF-solders require more thorough moisture removal.
    - ➢ Any remaining moisture will vaporize and create high vapor pressure levels within the PCB.
    - ➢ These vapor pressures can rupture the PCB matrix and separate PCB layers.

Vapor Pressure in PWB During Soldering



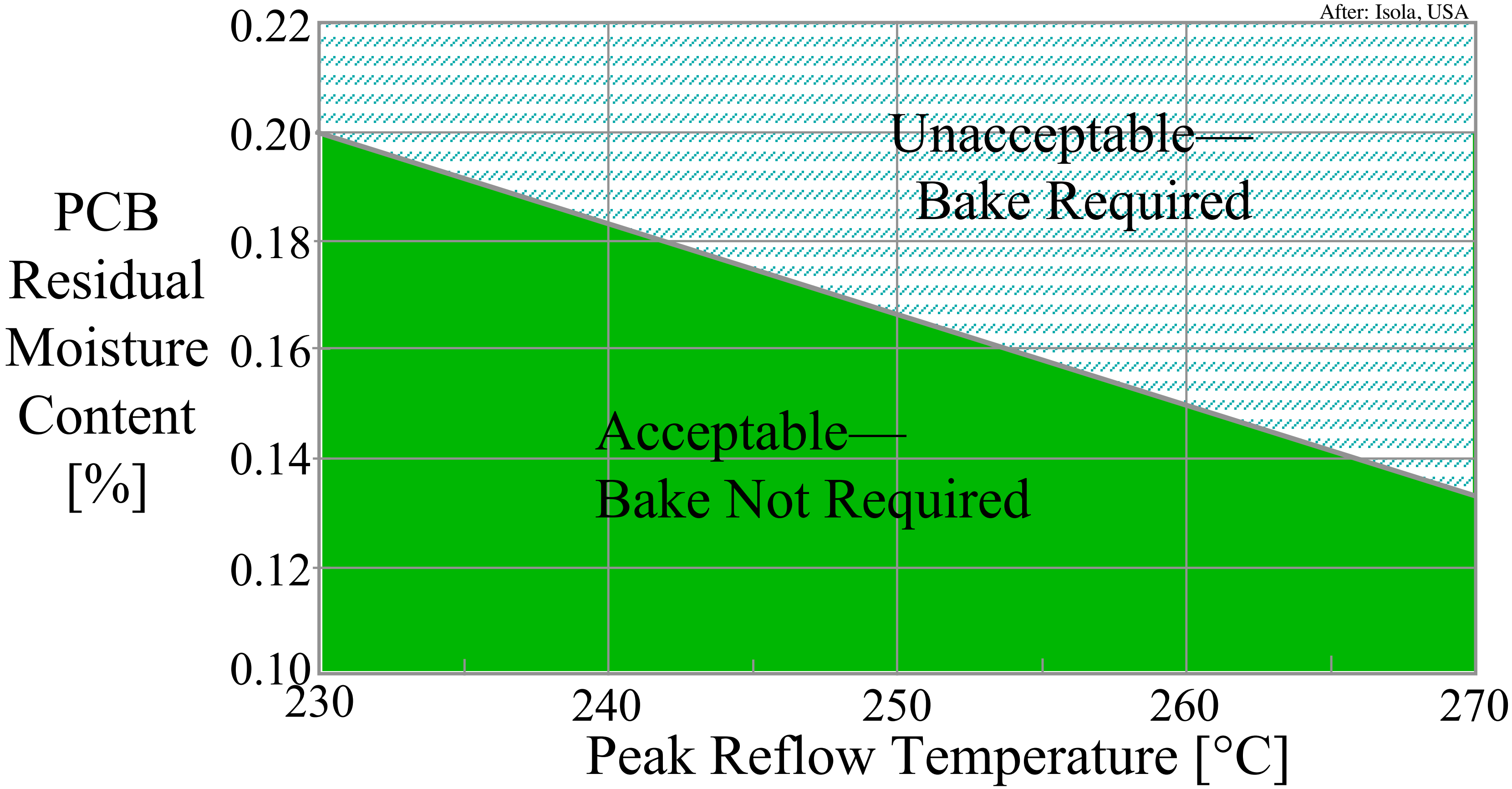
Water Vapor Pressure Induced PCB Layer Separation

Note: **Top photo is from SMT reflow process; bottom picture is from rework procedure.**



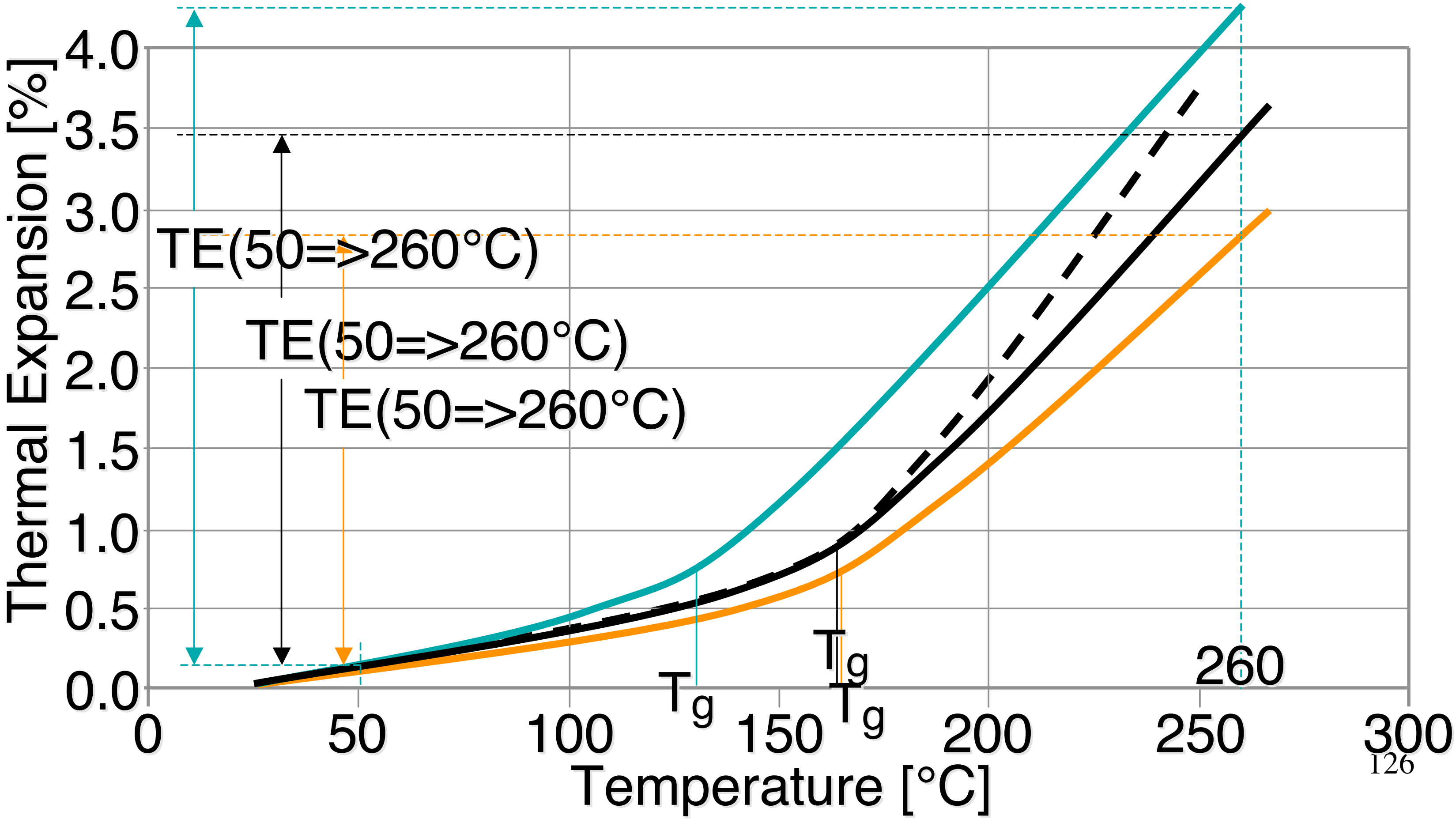
Courtesy of D. Mattix, Qualcomm Inc., USA

PCB Residual Moisture Content



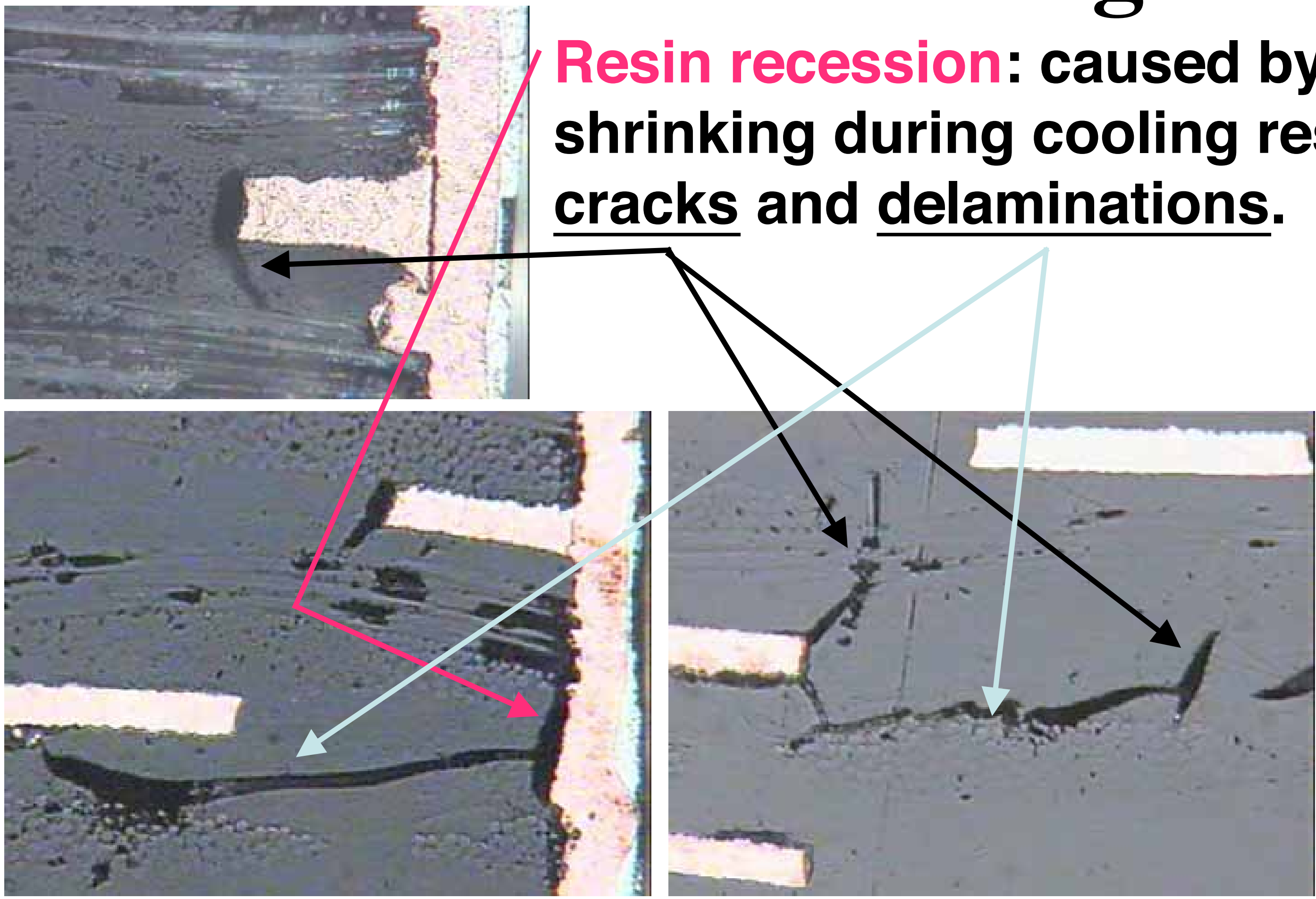
T_g's, CTE's & Thermal Expansion

It is the combined effect of the glass transition temperature and the above T_g coefficient of thermal expansion that determine the thermal expansion at soldering temperatures.



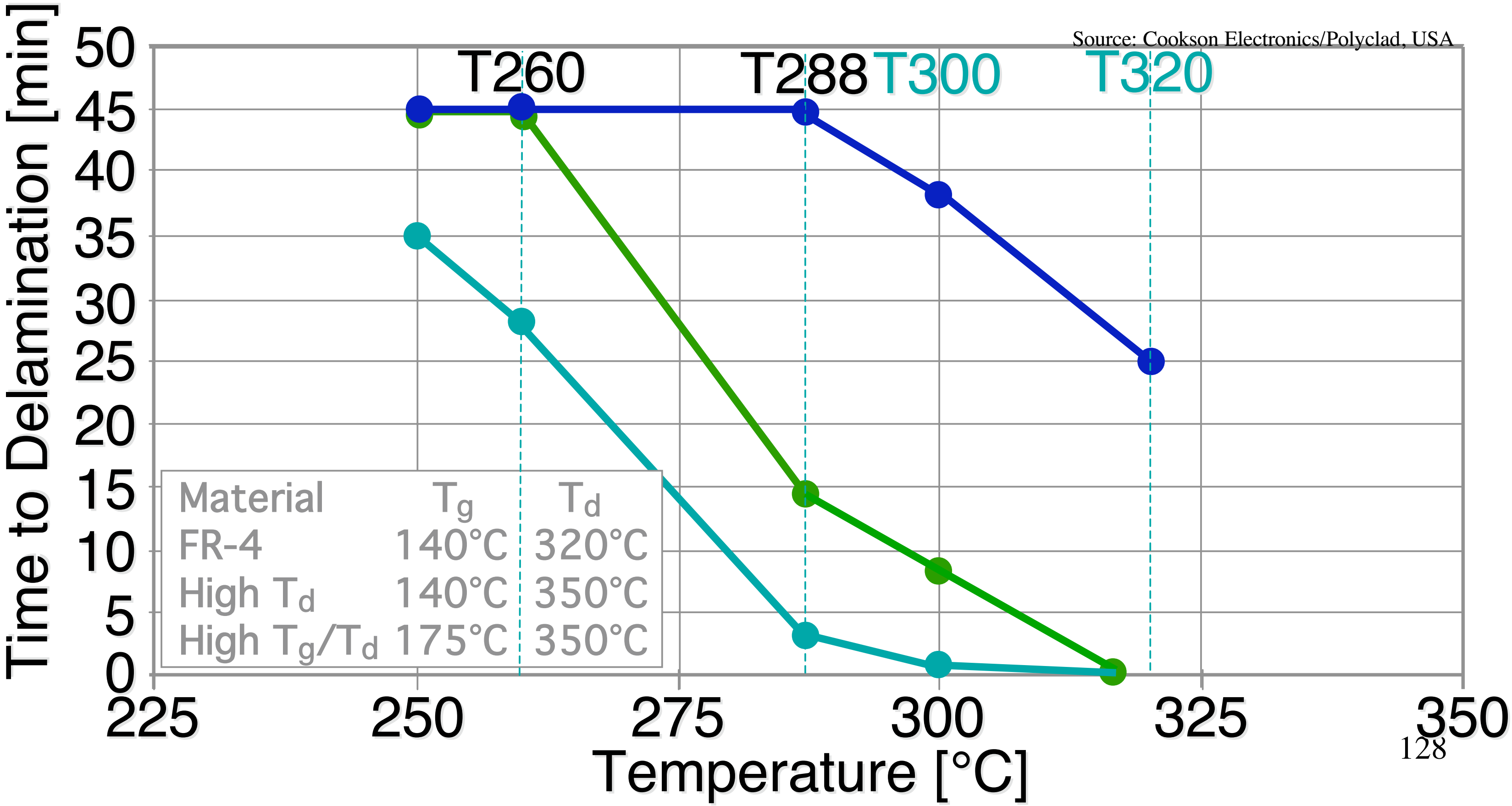
Cracks/Delaminations Caused By Resin Recession During Rework

Resin recession: caused by the resin shrinking during cooling resulted in cracks and delaminations.



Time to Delamination

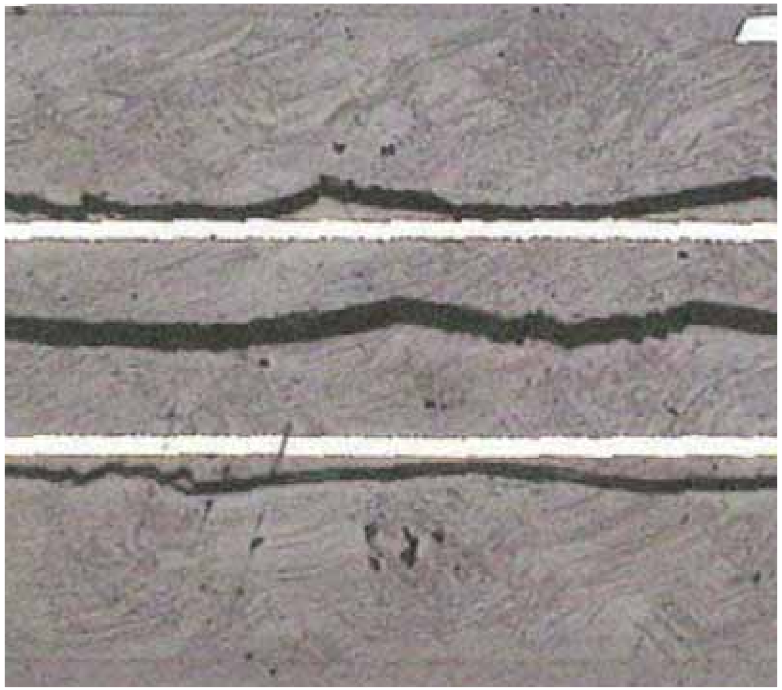
Thermal stability as measured by Thermo-Mechanical Analysis (TMA) on laminate.



Thermal Degradation/Decomposition

Massive delamination shown in 2 views; one to emphasize the delamination, one to show the structure details.

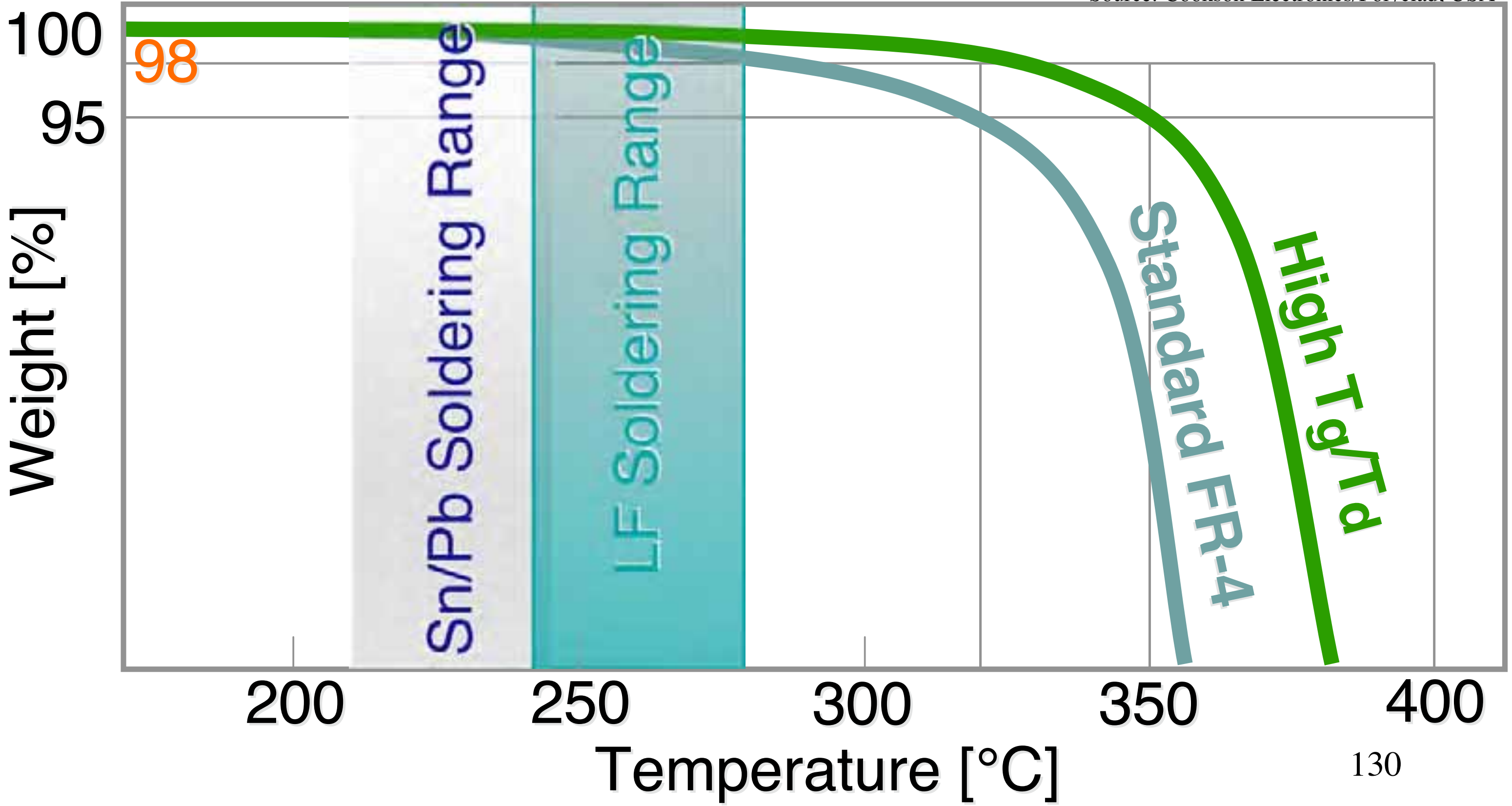
Source: Cookson Electronics/Polyclad, USA



Decomposition Temperature, T_d

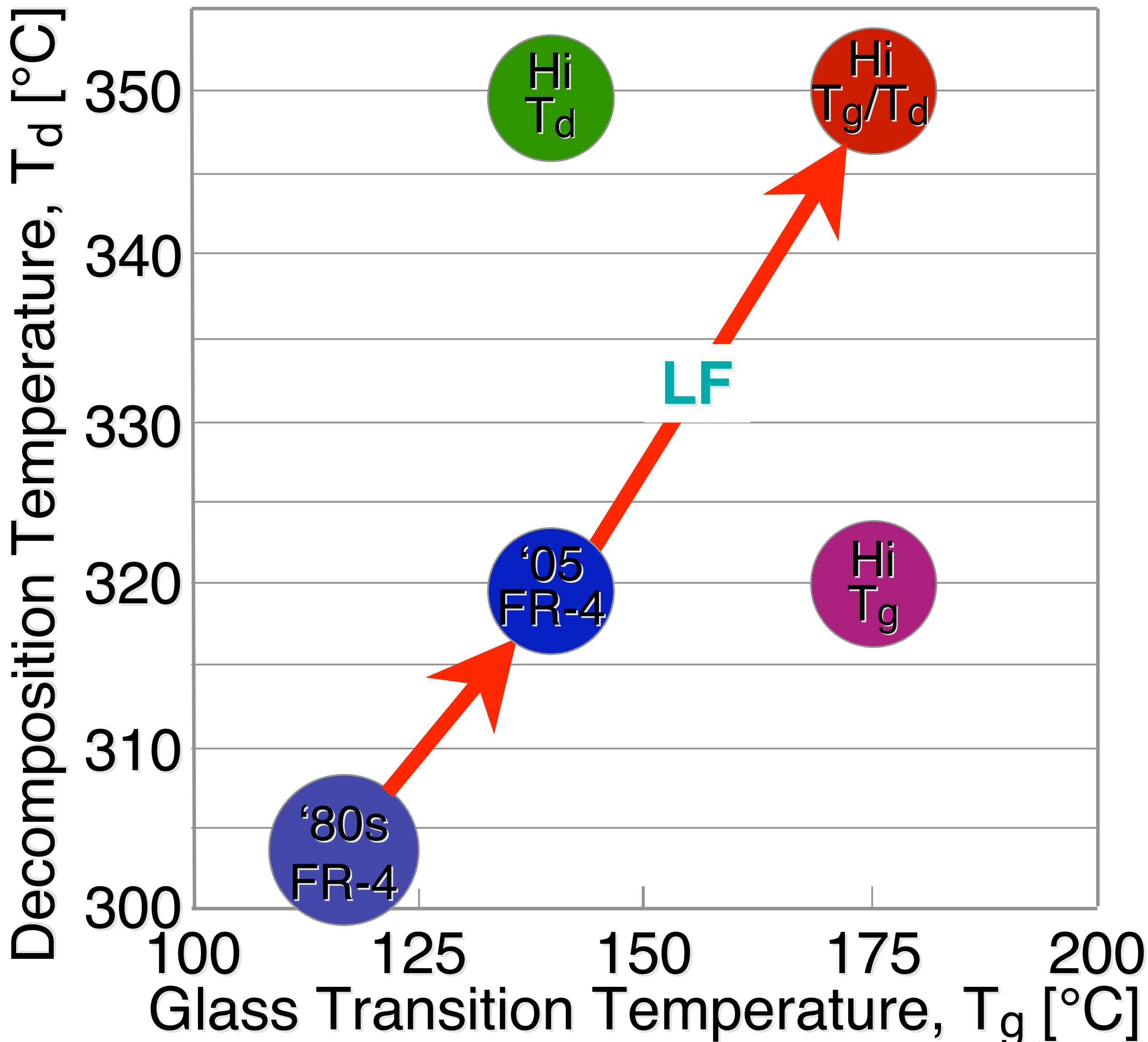
T_d is defined as the temperature at which 2% [T_d(2%)] and 5% [T_d(5%)] weight loss occurs at a heating rate of 10°C/min. Even a 2% weight loss indicates significant degradation of the resin. This weight loss signals an irreversible deterioration of the material.

Source: Cookson Electronics/Polyclad, USA



Thermal Stability/High Reliability

‘Standard’ FR-4 has improved since the 1980’s. With the advent of the soldering processes necessary for lead-free soldering, further significant improvement will be needed.



Proposed
Soldering Temperature Impact Index

The problem with the current IPC slash sheets is that they are to complex to be of practical use for the PCB designers. The STII is designed to give the designer an immediate feed-back whether or not to further consider this slash sheet product

$$\mathbf{STII = \frac{Tg + Td}{2} - [\%\ thermal\ expansion\ 50\ to\ 260°C] \times 10}$$

Examples: Tg =140°C, Td(5%) = 320°C, 4.3% TE 50⇒260°C

➢ STII = 187

Tg =175°C, Td(5%) = 350°C, 4.0% TE 50⇒260°C

➢ STII = 223

Possible range of STII ~150 to 250; specify STII ≥ 215 (for thin PCBs STII ≥ 205 is likely sufficient).

STII-Values for Some Laminate Materials

Vendor	Grade	Tg(TMA)	Td(5%)	TE(50-260°C)	STII
TUC	TU-622-5	135°C	310°C	4.1%	181
ISOLA	IS400	135°C	330°C	3.0%	202
NELCO	N4000-7	150°C	330°C	3.7%	203
TUC	TU-662	145°C	340°C	3.4%	209
ISOLA	FR250HR	140°C	350°C	3.4%	211
TUC	TU-722	172°C	330°C	3.5%	216
ISOLA	IS410	170°C	350°C	3.5%	225
NELCO	N4000-11	170°C	345°C	3.2%	225
TUC	TU-752	170°C	350°C	2.7%	233
ISOLA	370HR	170°C	350°C	2.7%	233
NELCO	N4000-12	180°C	370°C	3.6%	239
NELCO	N4000-13	200°C	365°C	3.5%	247
ISOLA	IS500	170°C	400°C	2.8%	257
TUC	TU-842	170°C	390°C	2.1%	259

Source: Engelmaier, W., WHITE PAPER: Recommendations for PCB FAB Notes and Specifications in Printed Circuit Board Drawings for SnPb and Lead-Free Soldering Assemblies, the Qualification of PCB Shops and Activities to Assure Continued Quality."

IPC-4101B

For the six (6) "Lead-Free Compatible" slash sheets :

Slash Sheet	Keyword			Tg	Td	TE(50⇨260°C)	STII
	LF	Hi Td	Lo zCTE	[°C]	[°C]	[%]	
/ 99	√	√	√	≥150	≥325	≤3.5	≥202
/101	√		√	≥110	≥310	≤4.0	≥170
/121	√		√	≥110	≥310	≤4.0	≥170
/124	√	√	√	≥150	≥325	≤3.5	≥202
/126	√	√	√	≥170	≥340	≤3.0	≥225
/129	√	√	√	≥170	≥340	≤3.0	≥225
LF	√	√	√	≥160	≥335	≤3.2	≥215

Remembering , that STII ≥215 is indicated for lead-free process compatibility with STII ≥205 likely sufficient for PCBs ≤50 mils thick.

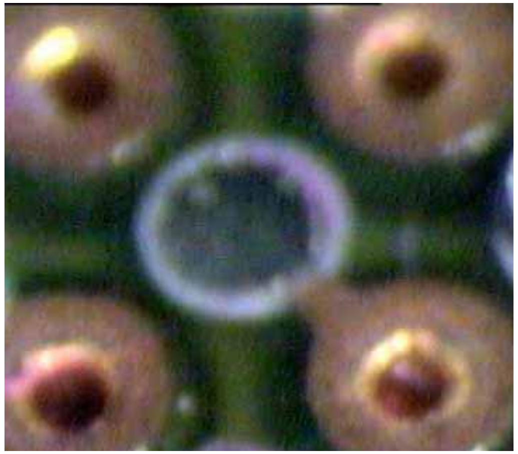
IPC-4101B

For the six (6) “Lead-Free Compatible” slash sheets :

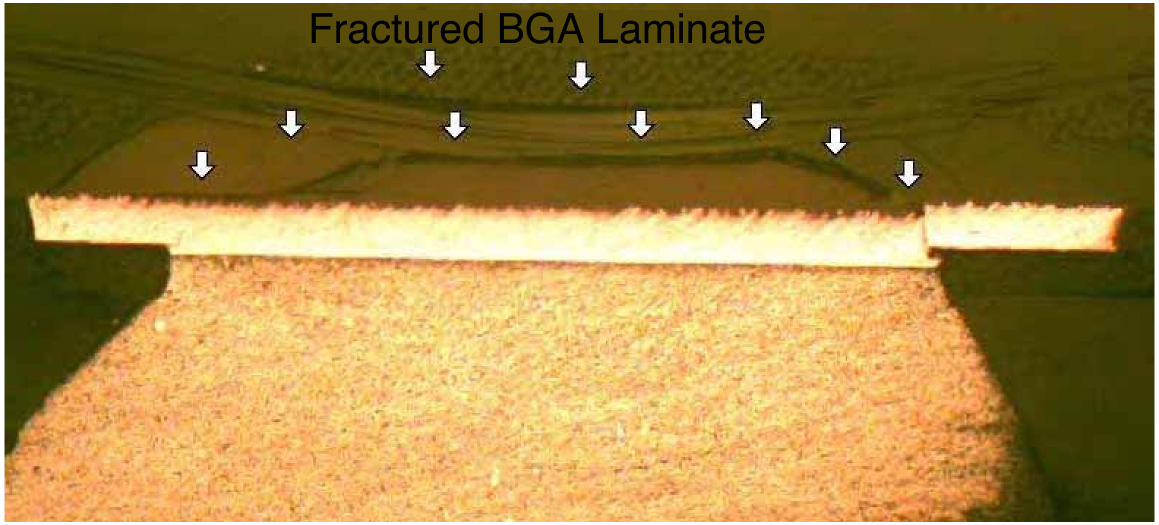
Slash Sheet	Keyword			Tg	Td	TE(50⇨260°C)	STII
	LF	Hi Td	Lo zCTE	[°C]	[°C]	[%]	
/ 99	√ Limited	√ NO	√ Limited	≥150	≥325	≤3.5	≥202
/101	√ NO		√ NO	≥110	≥310	≤4.0	≥170
/121	√ NO		√ NO	≥110	≥310	≤4.0	≥170
/124	√ Limited	√ NO	√ Limited	≥150	≥325	≤3.5	≥202
/126	√	√	√	≥170	≥340	≤3.0	≥225
/129	√	√	√	≥170	≥340	≤3.0	≥225
LF	√	√	√	≥160	≥335	≤3.2	≥215

Remembering , that STII ≥215 is indicated for lead-free process compatibility with STII ≥205 likely sufficient for PCBs ≤50 mils thick.

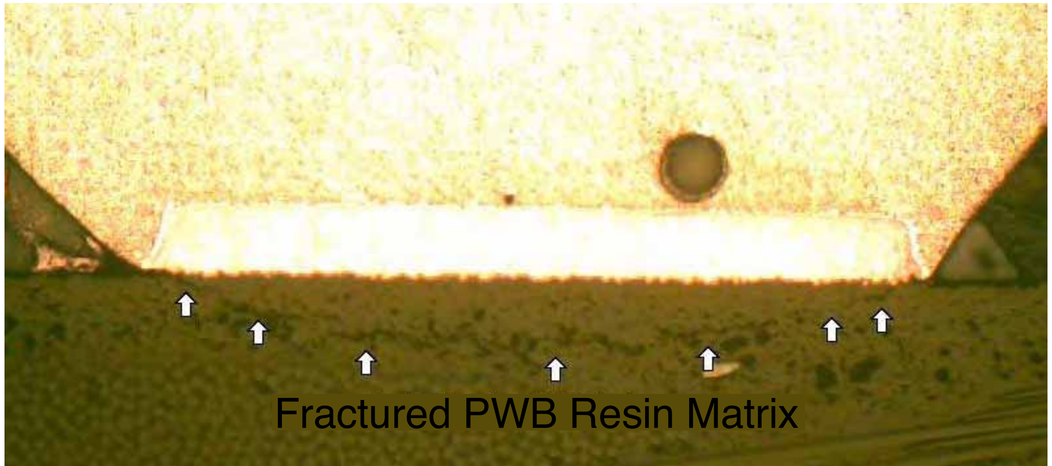
Pad Cratering (1)



Crater left behind in PWB



Courtesy of Bob Willis, UK

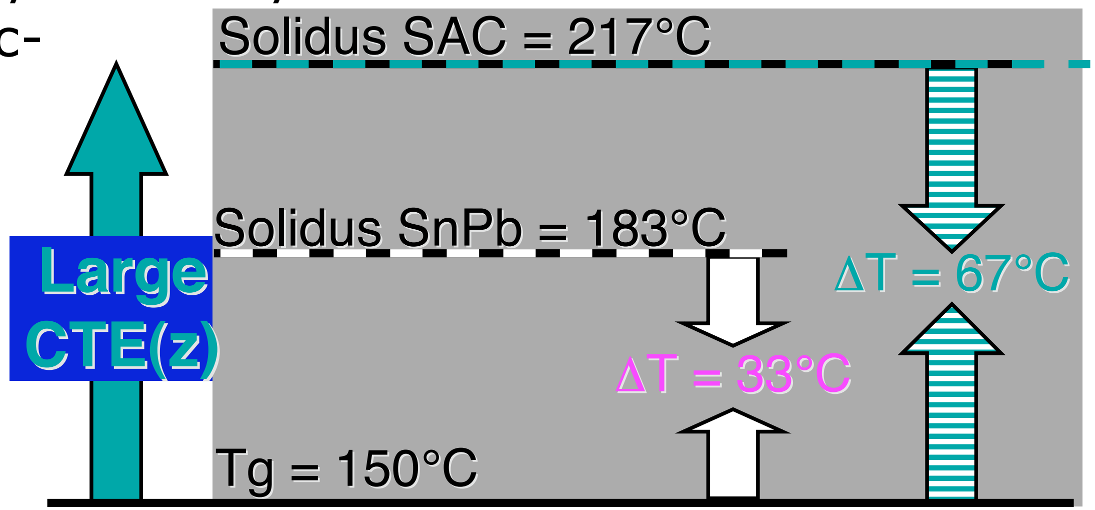


Courtesy of Cheryl Tulkoff, National Instruments, USA

Pad Cratering (2)

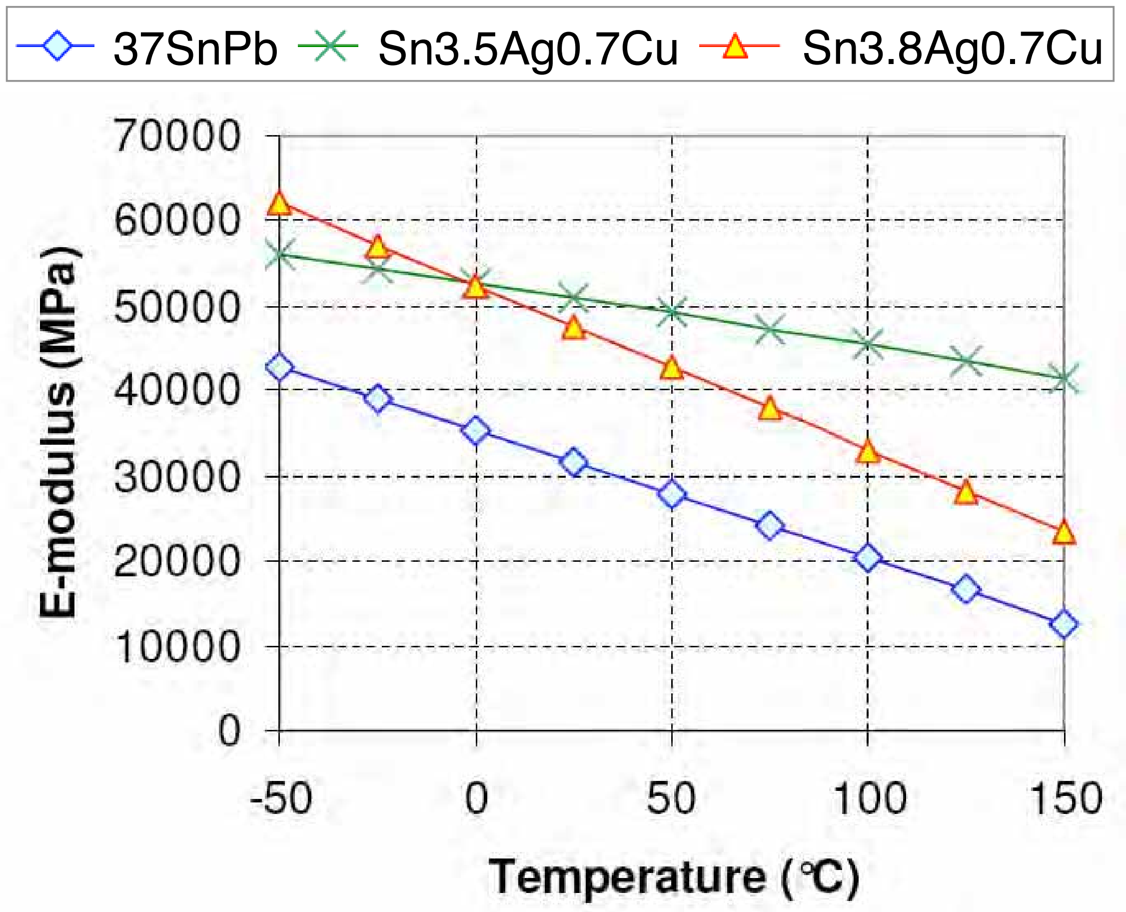
Pad Cratering is caused by a combination of underlying conditions.

- The SAC solders are about 40% stiffer than SnPb solders—this results in higher stresses at the pads.
- SAC solders have a Solidus of ~217°C vs. 185°C for SnPb—this results in about double the ΔT and thus double the expansion mismatch, given a Tg=150°C.
- The soldering temperatures needed for SAC solders drive the PCB base materials away from dicy-cured resins and towards the more brittle phenolic-cured 'RoHS-capable' resins.
- This results in higher stresses on the pads by about a factor of 3 to 4.



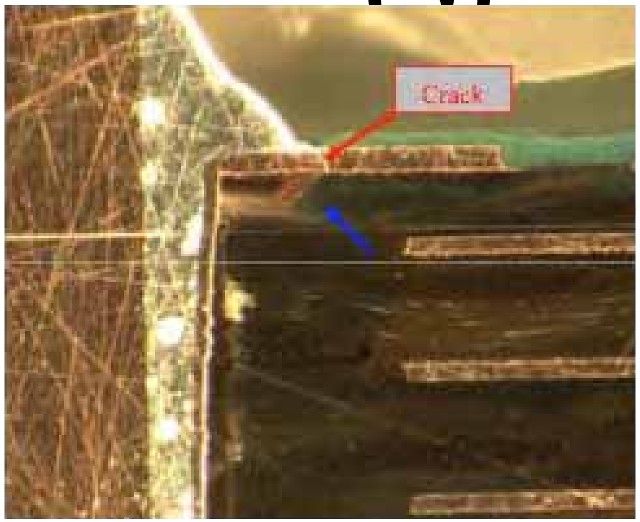
Modulus of Elasticity for Some SAC SnPb Solders

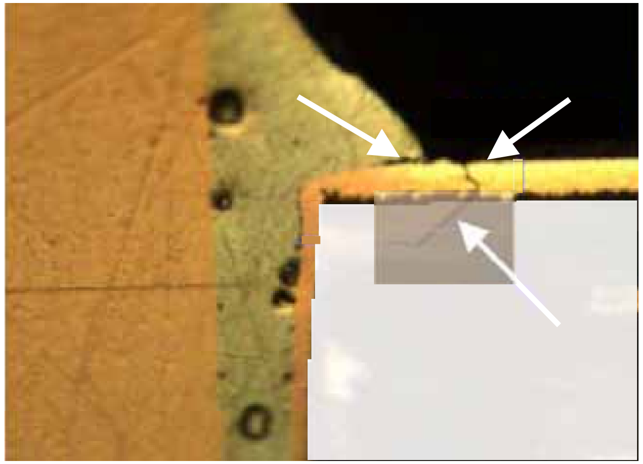
<u>Note</u>: Modulus for SAC solder is much higher than those of SnPb; this indicates a much higher stress response to any loading.

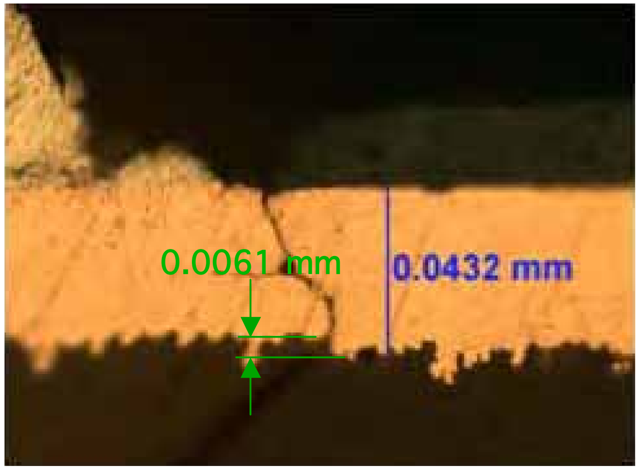


Source: A. Schubert, et al, Germany

Pad Cratering and Trace Fractures (3)







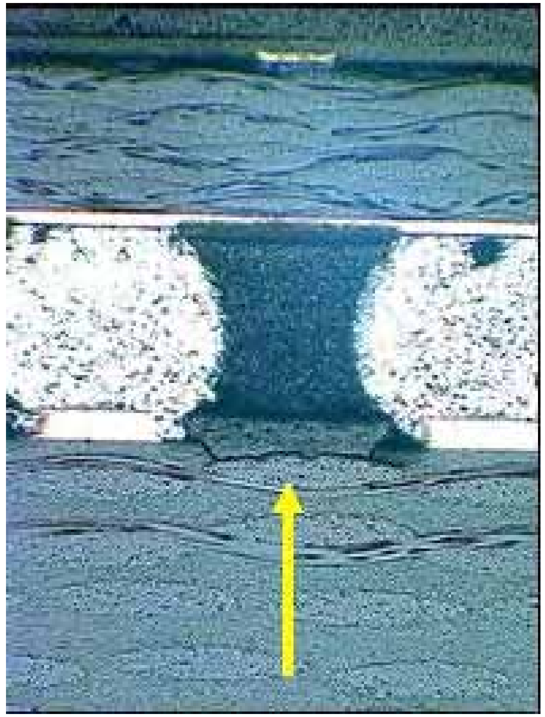
Courtesy of Harman/Becker, USA

Note: The thermal expansion mismatch causing the pad cratering also caused the fracture of a connecting trace.

In-Between Pad Cratering (4)

Complete underfill with Loctite® 3568 w/
120 minute cure at 125°C,
Cured underfill: E= 1.4 N/mm2
[0.0014 GPa, 200 psi],
CTE=40 ppm/°C/
->Tg=70°C/145 ppm/°C

Note: Because of the very low compressibility of these resin types, the much higher CTEs both below and above Tg, as compared to the solder balls, combined with the large temperature excursion during soldering are the root causes of this failure.



Source: Dave Hillman, Rockwell Collins, USA

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Component Structures : Load Drivers (1)

- Internal Water Vapor Pressure
  - Absorbed water must be baked out of the component. If too much moisture remains in component during solder reflow, significant vapor pressure is created inside the component
- Potential Problem
  - “Popcorning” of component body
    - ➢Die cracking/bond delamination

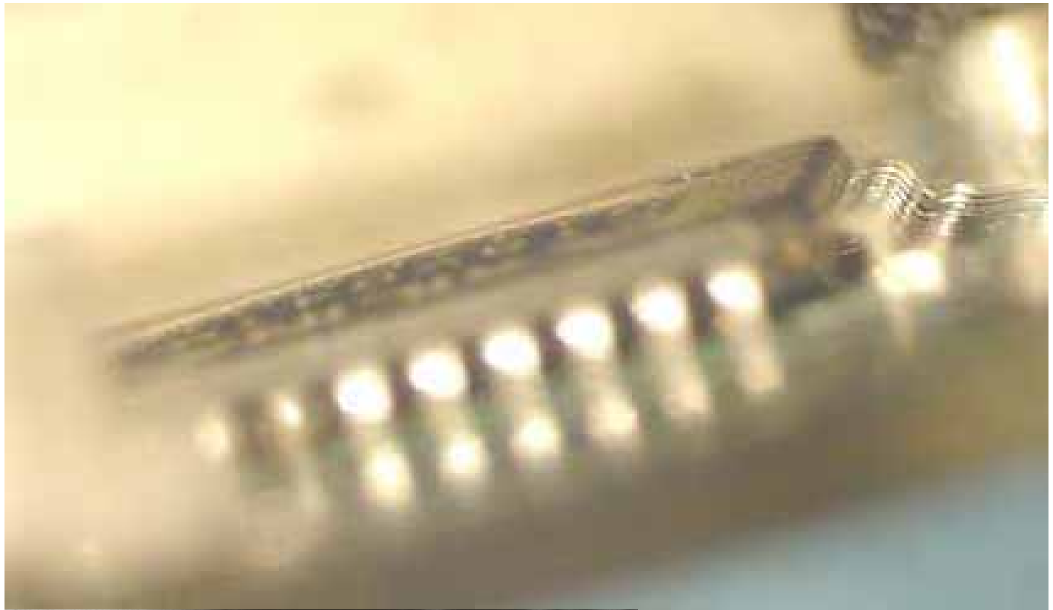
Component Structures : Load Drivers (2)

- Thermal Expansion Mismatches
  - Die [2.8 ppm/^{o}C] vs. component substrate [11-28 ppm/^{o}C]
  - Die vs. component substrate vs. heat sink [18 ppm/^{o}C]
  - Die vs. encapsulant [20-28 ppm/^{o}C]
- Potential Problem
  - Die bond interfacial stress
    - ➢ Die cracking/bond delamination
  - Component warpage
    - ➢ Soldering pad ripped out of resin matrix

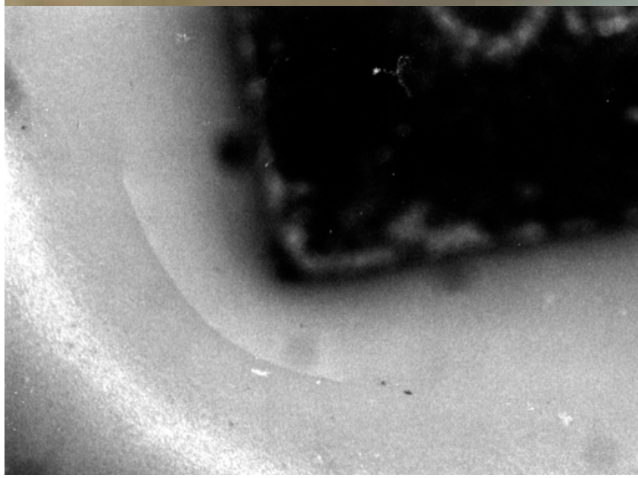
Popcorning: Surface Bulge

The component top shows a pronounced bulge from popcorning.

Note: That means there are internal and possibly external cracks.



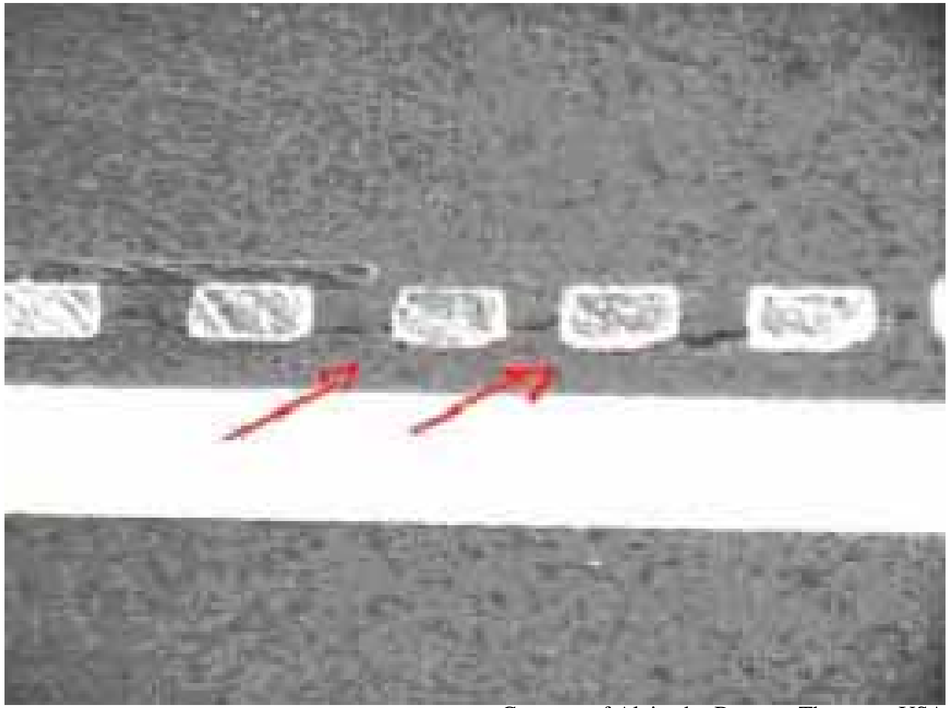
Courtesy of a colleague, USA



Popcorning: Cross-Section

This shows a x-section of a popcorned component with internal cracks.

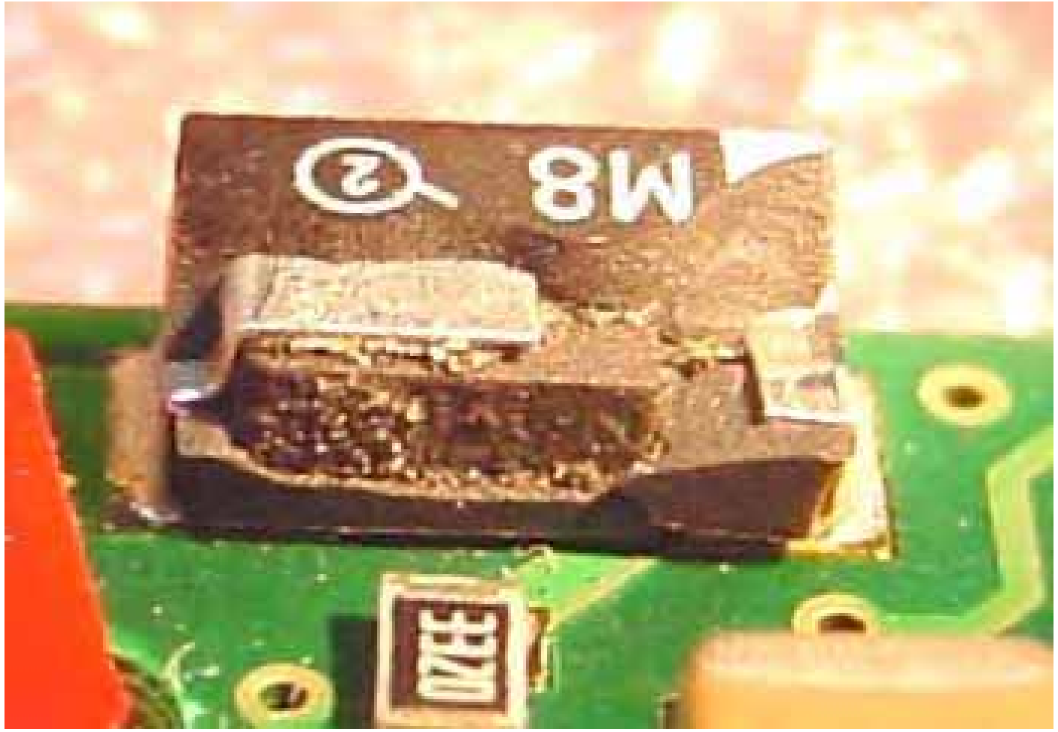
<u>Note:</u> It is possible for this cracks to extend to component surface.



Courtesy of Alejandro Becerra, Thomson, USA

Exploded Tantalum Capacitor

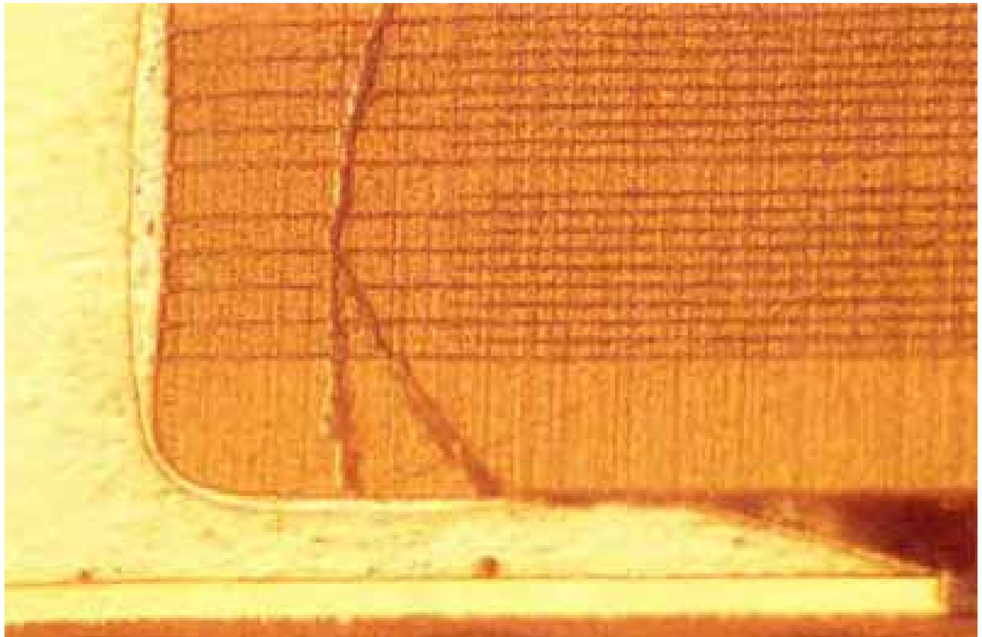
This component was destroyed during lead-free reflow soldering, venting steam when bursting.



Courtesy of John Maxwell, USA

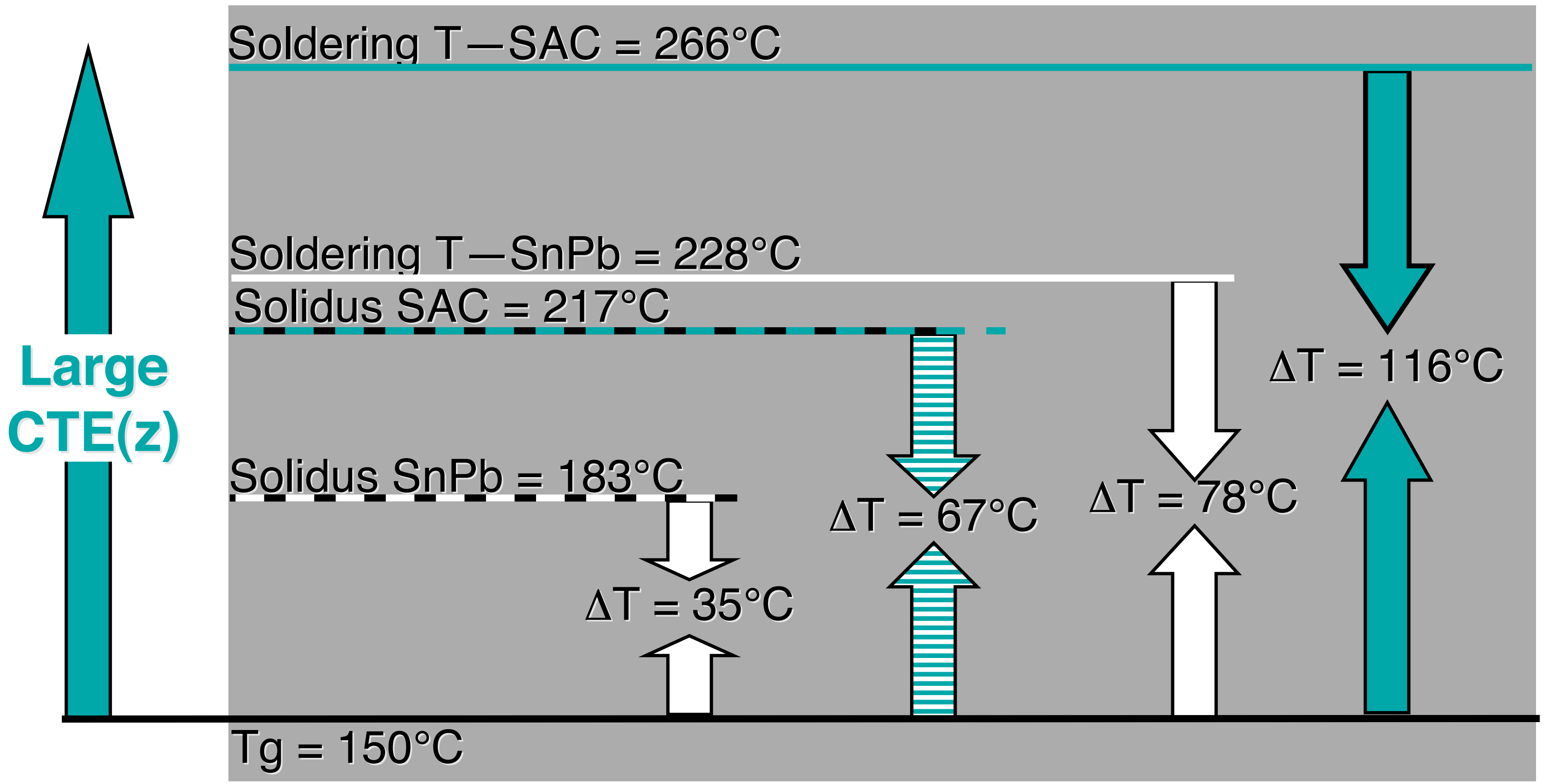
Cracked Components

- Chip components (resistors and capacitors) have a higher propensity to crack with LF-solders, because the solder solidification occurs at higher temperatures and together with the slower creep rates lead to higher stresses due to the thermal expansion mismatches.

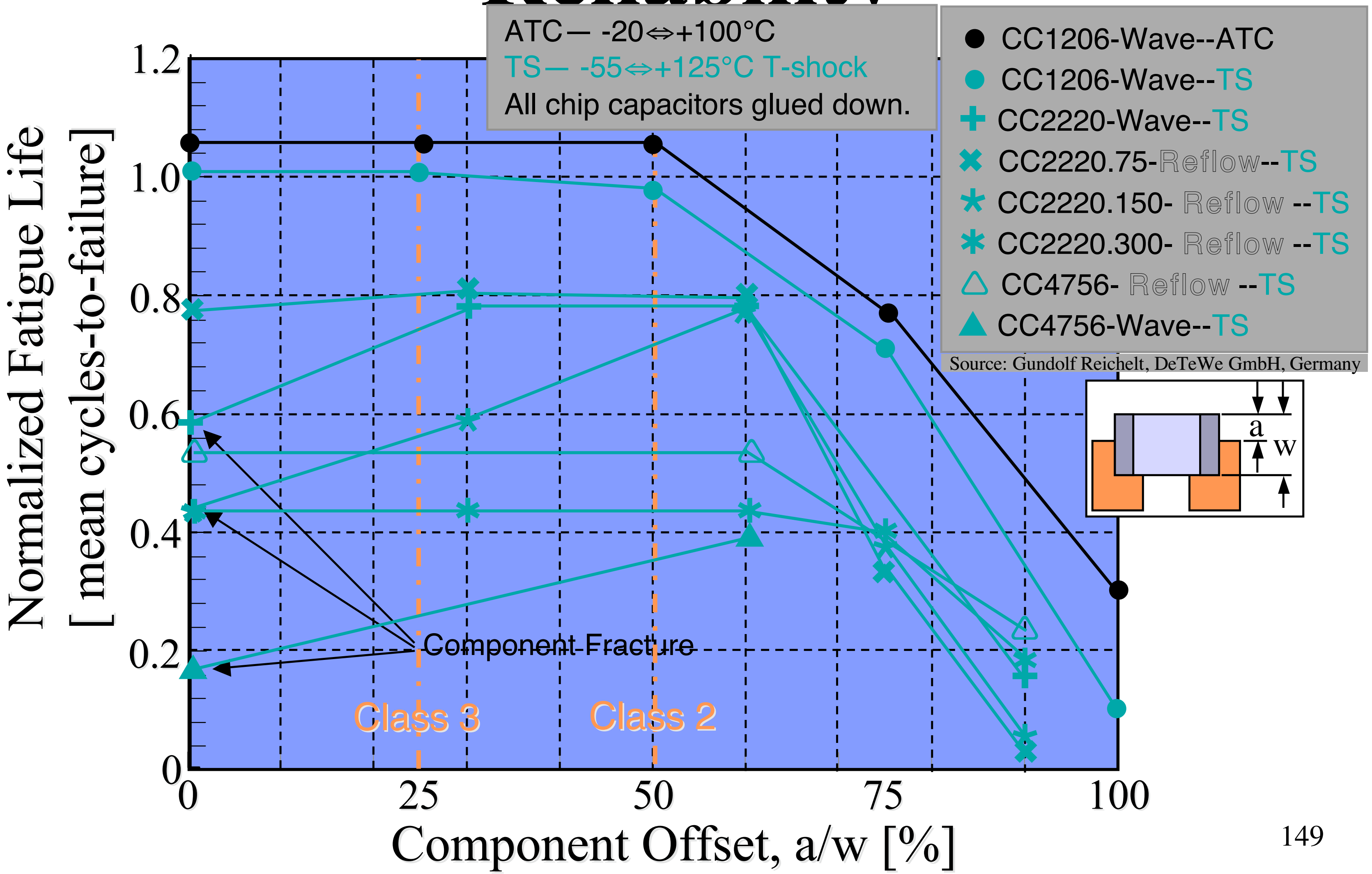


Courtesy of Bob Willis, UK

Important ΔT's for SnPb vs. SAC



Component Offset: Quality vs. Reliability



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Reliability Assurance Test for Sn/Pb Solder Joints

- Accelerated Temperature Cycling
  - According to IPC-9701 “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments” & IPC-SM-785 “Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments.”
  - Based on large data base and verified creep-fatigue models acceleration factors to field reliability can be determined.
  - Establishes capability of solder alloys tested to withstand cyclic creep-fatigue.

IPC-9701 : Scope (1)

... establishes standardized test methods to evaluate the performance and reliability of SM solder attachments;

...establishes levels of performance and reliability of the solder attachments of surface mount devices to provide confidence that the design and the manufacturing/assembly processes create a product that is capable of meeting its intended goals;

...provides an approximate means of relating the results from these performance tests to the reliability of solder attachments for the use of electronic products with Sn/Pb solders.

IPC-9701 : Scope (2)

... the standardized test method is generic; it is NOT SnPb or LF-solder specific;

…while the levels of performance are generic, it has become evident from the determined creep-fatigue behavior of LF-solders, that the performance levels need to be modified to take the slower creep rates into account;

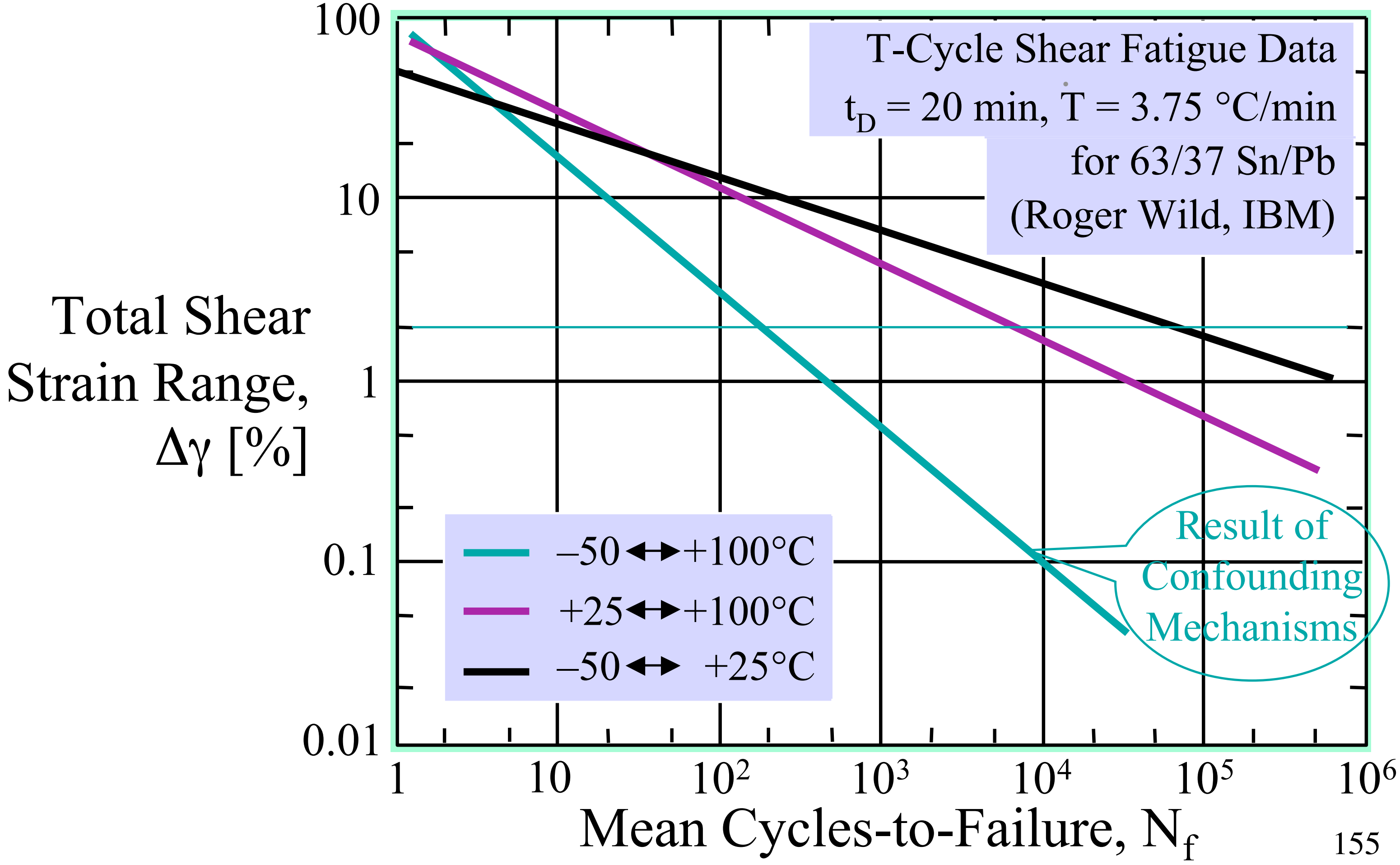
…in the absence of a creep-fatigue model for LF-solders, a performance standard for LF-solder attachments cannot be established as yet—IPC-9701A for LF-solders is a guidelines document;

…in the absence of a creep-fatigue model for LF-solders, the reliability of LF-solder attachments for the use of electronic products cannot be established as yet.

IPC-9701 Thermal Cycling Test Levels

Test Level	T(min)	T(max)	ΔT	Remarks
TC1	**0°C**	**+100°C**	**100°C**	**Benchmark**
TC2	-25°C	+100°C	125°C	
TC3	-40°C	+125°C	165°C	Confounding Mechanisms Violate IPC-SM-785
TC4	-55°C	+125°C	180°C	
TC5	-55°C	+100°C	155°C	

IRAD Thermal Cycling Data



Thermal Excursions (Field Extremes)

Industry Standard IPC-SM-785

USE	Tmin	Tmax	ΔT	Cyl/Yr	Years	Acc.Fails
CONSUMER	0°C	+60°C	35°C	365	1-3	~1%
COMPUTERS	+15°C	+60°C	20°C	1460	~5	~0.1%
TELECOMM	-40°C	+85°C	35°C	365	7-20	~0.01%
COMMERCIAL AIRCRAFT	-55°C	+95°C	20°C	365	~20	~0.001%
INDUSTRIAL & AUTOMOTIVE-PASSENGER	-55°C	+95°C	60°C	365	~10	~0.%1
MILITARY GROUND&SHIP	-55°C	+95°C	60°C	365	~5	~0.1%
SPACE	-40°C	+85°C	35°C	8800	5-20	~0.001%
MILITARY AVIONICS	-55°C	+95°C	80°C	365	~10	~0.01%
AUTOMOTIVE-UNDER HOOD	-55°C	+125°C	100°C	1300	~5	~0.1%

LF o.k. (Consumer, Computers, Telecomm)

LF not recommended as yet (Commercial Aircraft through Automotive-Under Hood)

Thermal Excursions Mandated for 20-Year Life of F-22 Fighter Jet

Loading	Cycles	Tmin	Tmax	ΔT
ESS	10	-40°C	+70°C	110°C
ATP	10	+25°C	+70°C	45°C
Storage	550	+15°C	+37°C	22°C
Flight 1	1	-40°C	+85°C	125°C
:	:	:	:	:
Flight 27	929	+20°C	+85°C	65°C
:	:	:	:	:
Flight 36	1	+45°C	+85°C	40°C
Tarmac 1	1	-50°C	-47°C	3°C
:	:	:	:	:
Tarmac 14	260	+20°C	+33°C	13°C
:	:	:	:	:
Tarmac 20	1	+45°C	+58°C	13°C
TOTAL: 59	10,500	--	--	--

ONLY POSSIBLE WITH CREEP-FATIGUE MODEL

IPC-9701 Qualification Levels

Qualification Levels	Cycles	Remarks
NTC-A	200	Infant Mortality ONLY
NTC-B	500	
NTC-C	1,000	Preferred for TC2, TC3, & TC4
NTC-D	3,000	
NTC-E	6,000	**Preferred for Benchmark TC1**

DO NOT ASSURE THE SAME RELIABILITY LEVEL FOR LF-SOLDERS

Equivalent Product Field Cycles/ Acceleration Factors for Sn/Pb (1)

TEST LEVEL		EQUIVALENT FIELD CYCLES	
Test Level	Qualification Requirement	Field Cycle	Cycle Estimates
TC1: ΔT=100°C 0<->+100°C	NTC-D = 3,000 cycles	ΔT = 35°C +20<->+55°C t_D = 660 min	12,000
TC2: ΔT=125°C -25<->+100°C			17,000
TC3: ΔT = 165°C -40<->+125°C			33,000
TC4: ΔT = 180°C -55<->+125°C			37,000

ONLY POSSIBLE WITH CREEP-FATIGUE MODEL

Equivalent Product Field Cycles/ Acceleration Factors for Sn/Pb (2)

TEST LEVEL		EQUIVALENT FIELD CYCLES, ACCELERATION FACTORS				
Test Level	Qualification Requirement	ΔT [°C]	Dwell [min]	Cycle Estimates	AF(N)	AF(t)
TC1: 0<->+100°C ΔT = 100°C	NTC-E = 6,000 cycles	20	660	86,000	14.29	401.3
			60	180,000	30.05	84.0
		140	660	1,200	0.19	5.6
			60	1,900	0.31	0.9
TC4: -55<->+125°C ΔT = 180°C	NTC-C = 1,000 cycles	20	660	53,000	54.45	1484.6
			60	109,000	109.17	305.3
		140	660	720	0.72	20.2
			60	1,100	1.13	3.1

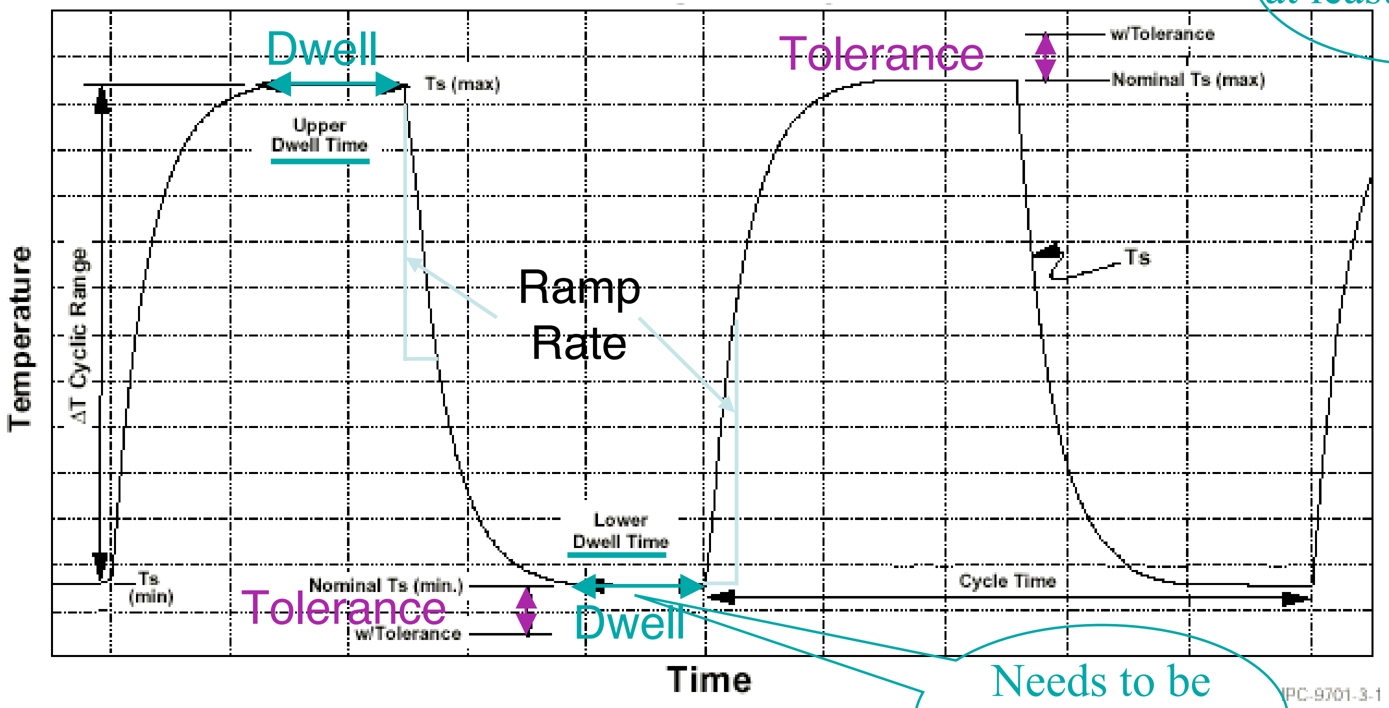
ONLY POSSIBLE WITH CREEP-FATIGUE MODEL

Test Temperature-Cycle: Dwells, Ramps, & Tolerances

Table 4-1 Temperature Cycling Requirements, Mandated and Preferred Test Parameters Within Mandated Conditions

Low Temperature Dwell Temperature Tolerance (preferred)	10 minutes +0/-10°C (+0/-5°C) [+0/-18°F (+0/-9°F)]
High Temperature Dwell Temperature Tolerance (preferred)	10 minutes +10/-0°C (+5/-0°C) [+18/-0°F(+9/-0°F)]
Temperature Ramp Rate	≤20°C [36°F]/minute

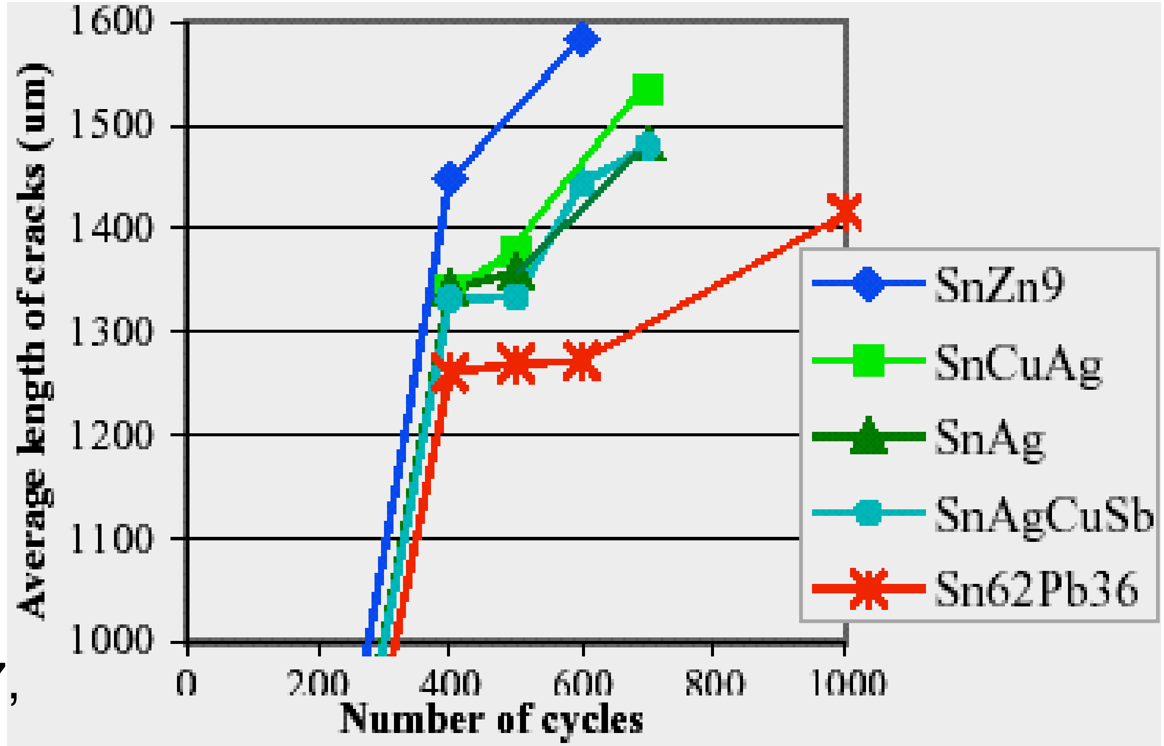
Needs to be at least 30 minutes



Needs to be at least 30 minutes

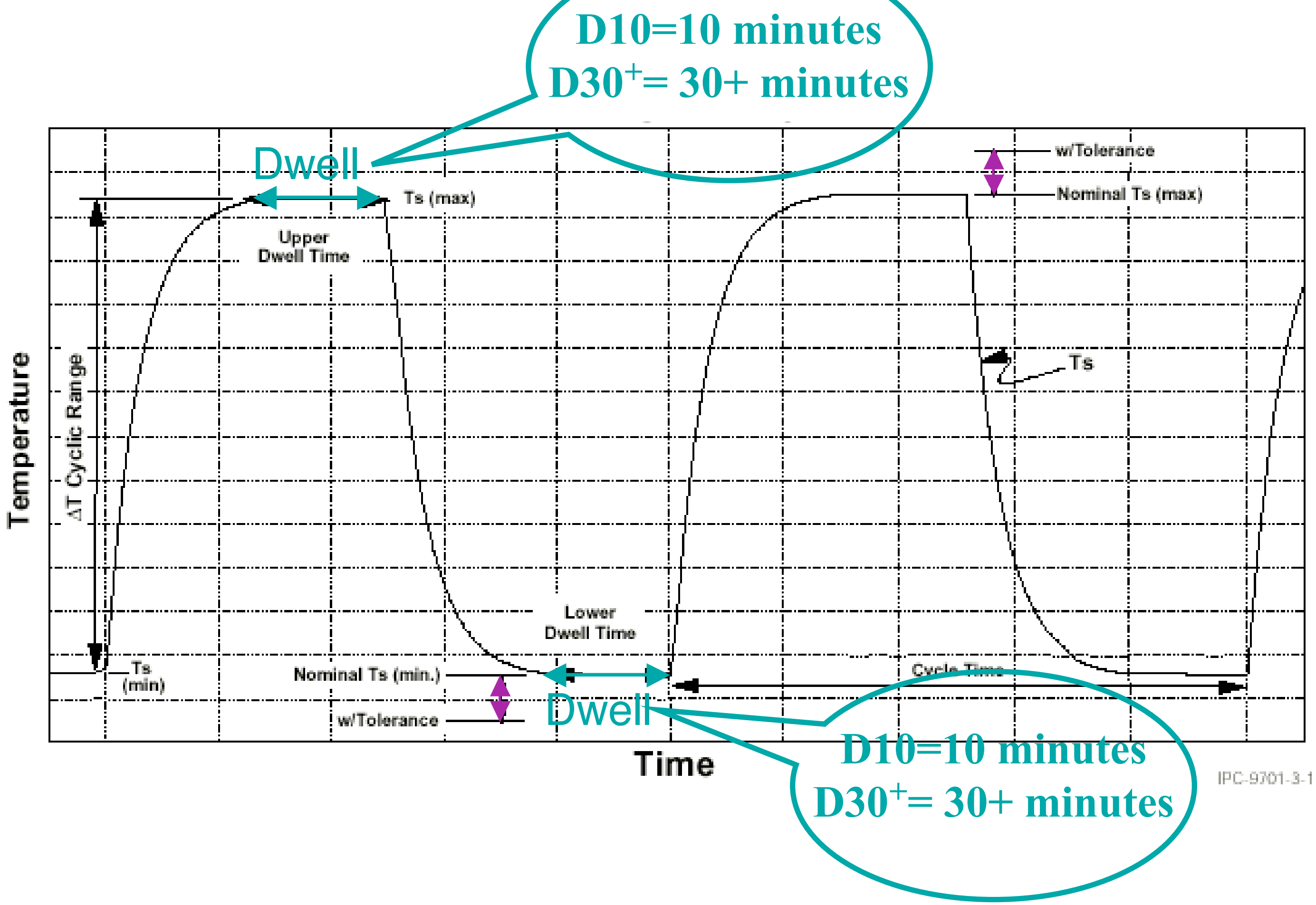
Comparative ATC Results

From European LEADFREE project:
LCCCs on FR-4;
ATC: -20°C {30’ dwell} ⇔ +120°C {10’ dwell};
Results: All solders showed cracking underneath LCCCs after 400 cycles, further crack propagation in fillets; the alloys tested were: Sn-Zn9, Sn-Ag3.8-Cu0.7, Sn-Ag3.5, Sn-Ag2.6-Cu0.8-Sb0.5 and Sn-Pb36-Ag2.



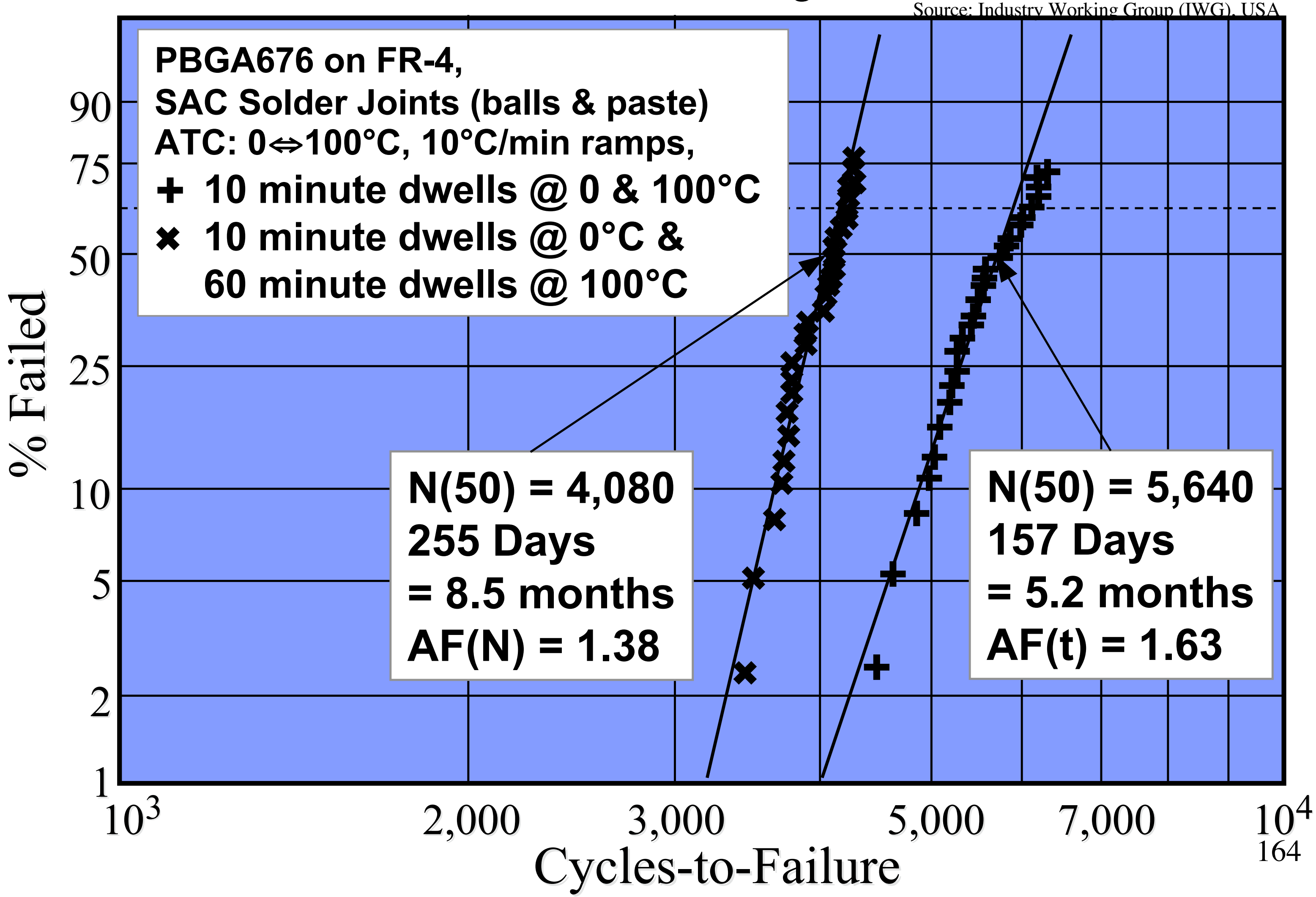
Courtesy of Günter Grossmann, EMBA Centre for Reliability, Switzerland

Test Temperature-Cycle: New IPC-9701A —D10 & D30+ Dwell Conditions

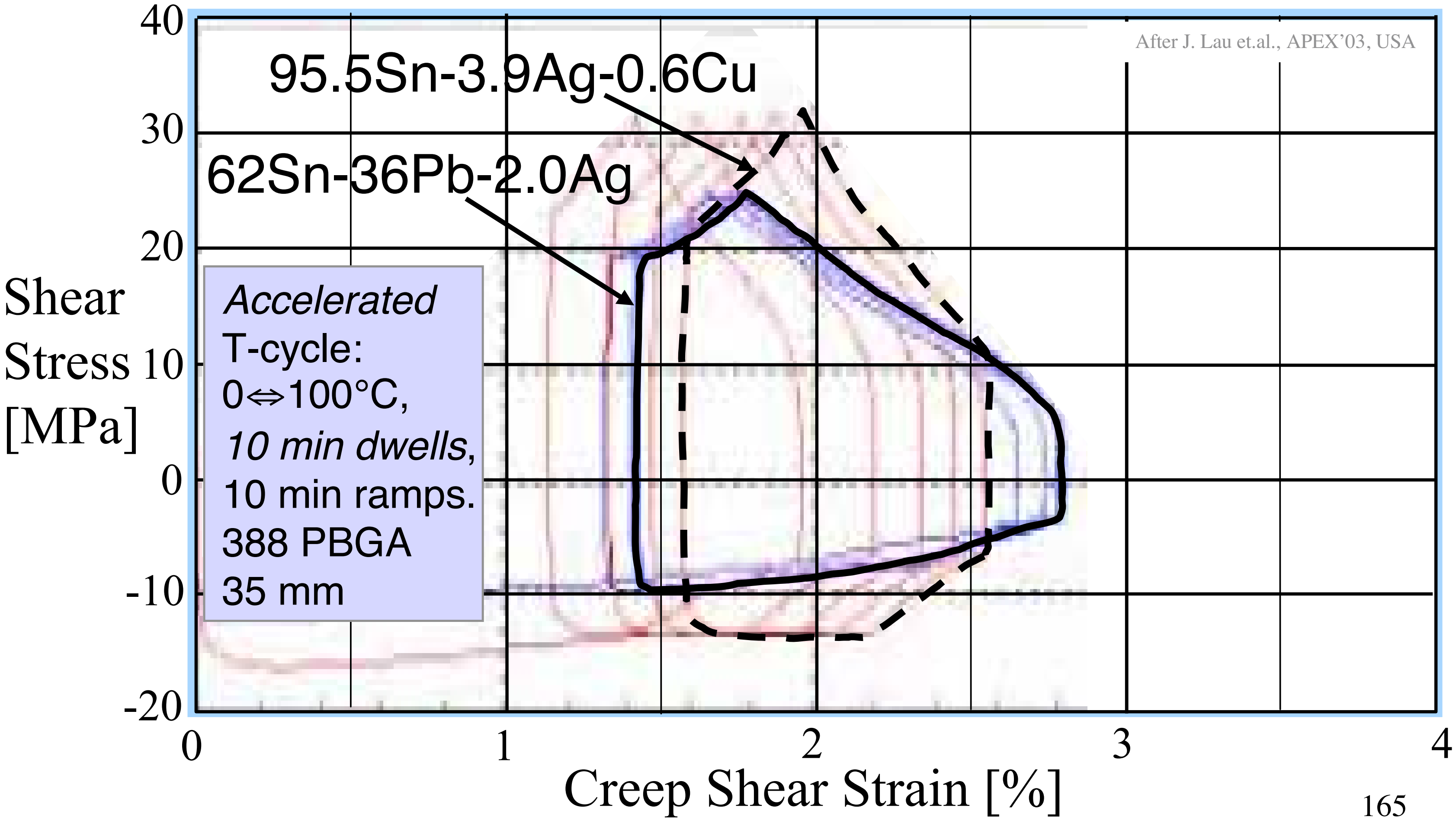


Acceleration Factors for Time and Cycles

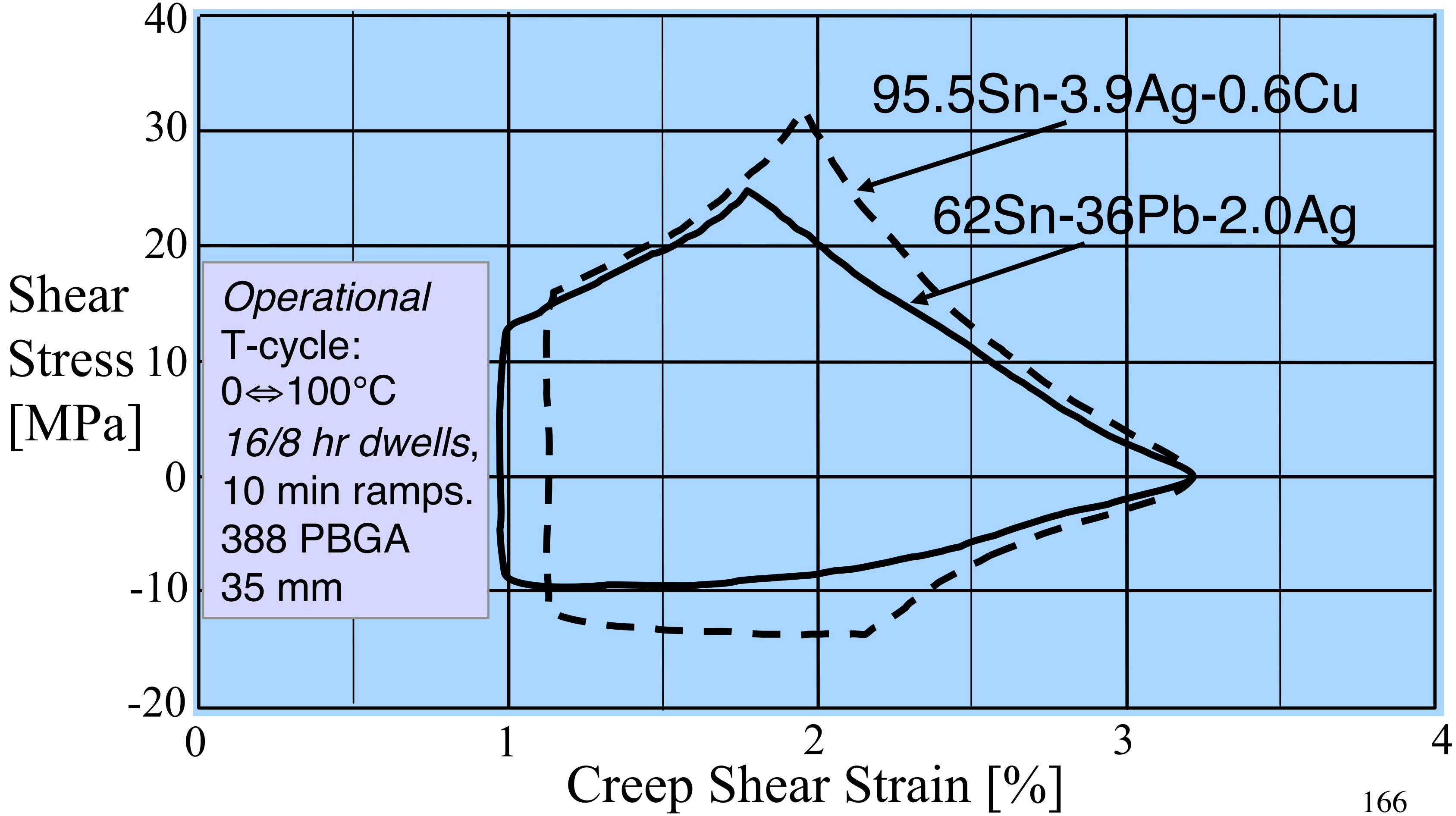
Source: Industry Working Group (IWG), USA



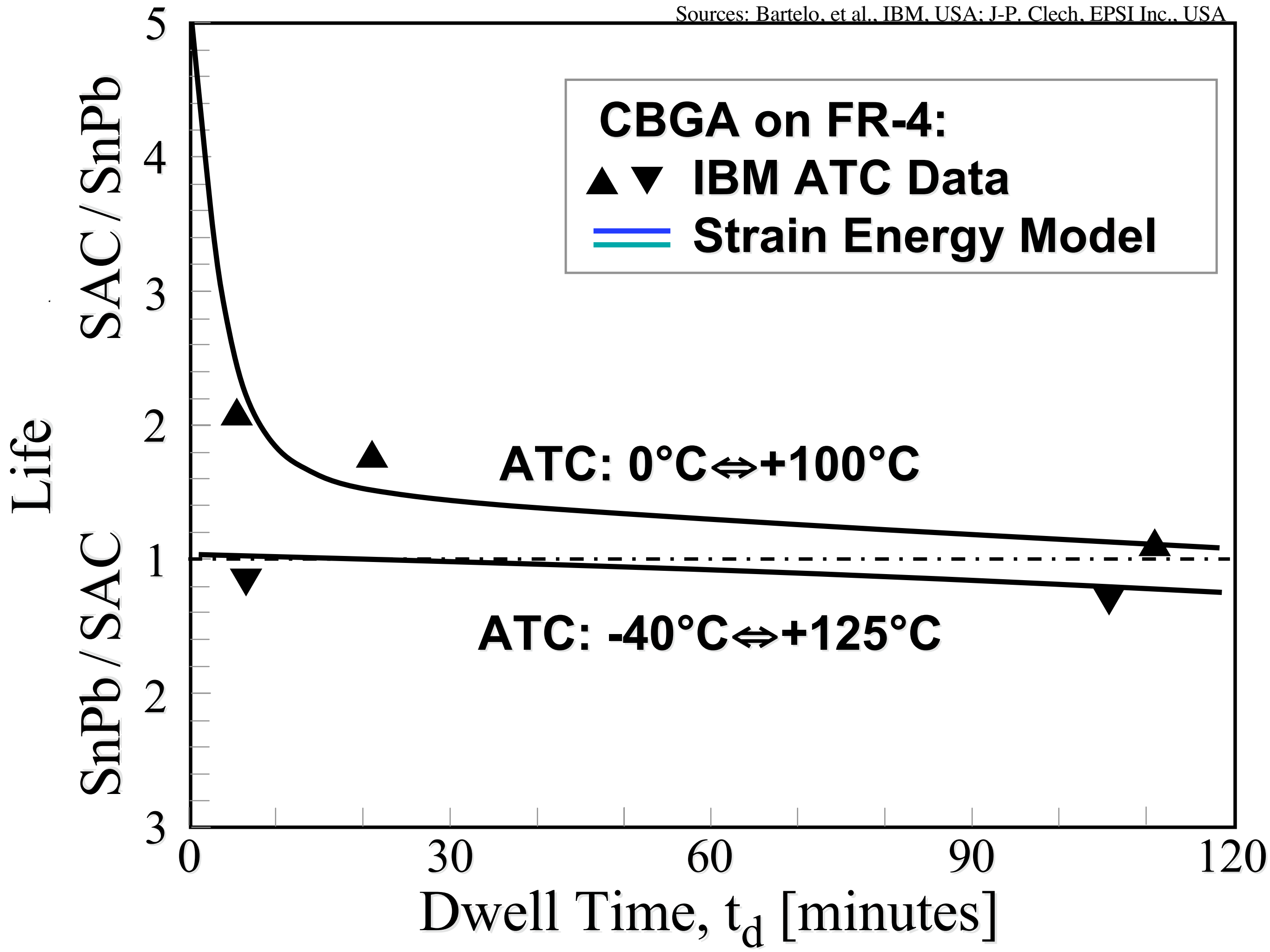
Fatigue Cycle Hysteresis Loops SAC vs. Sn/Pb Solder



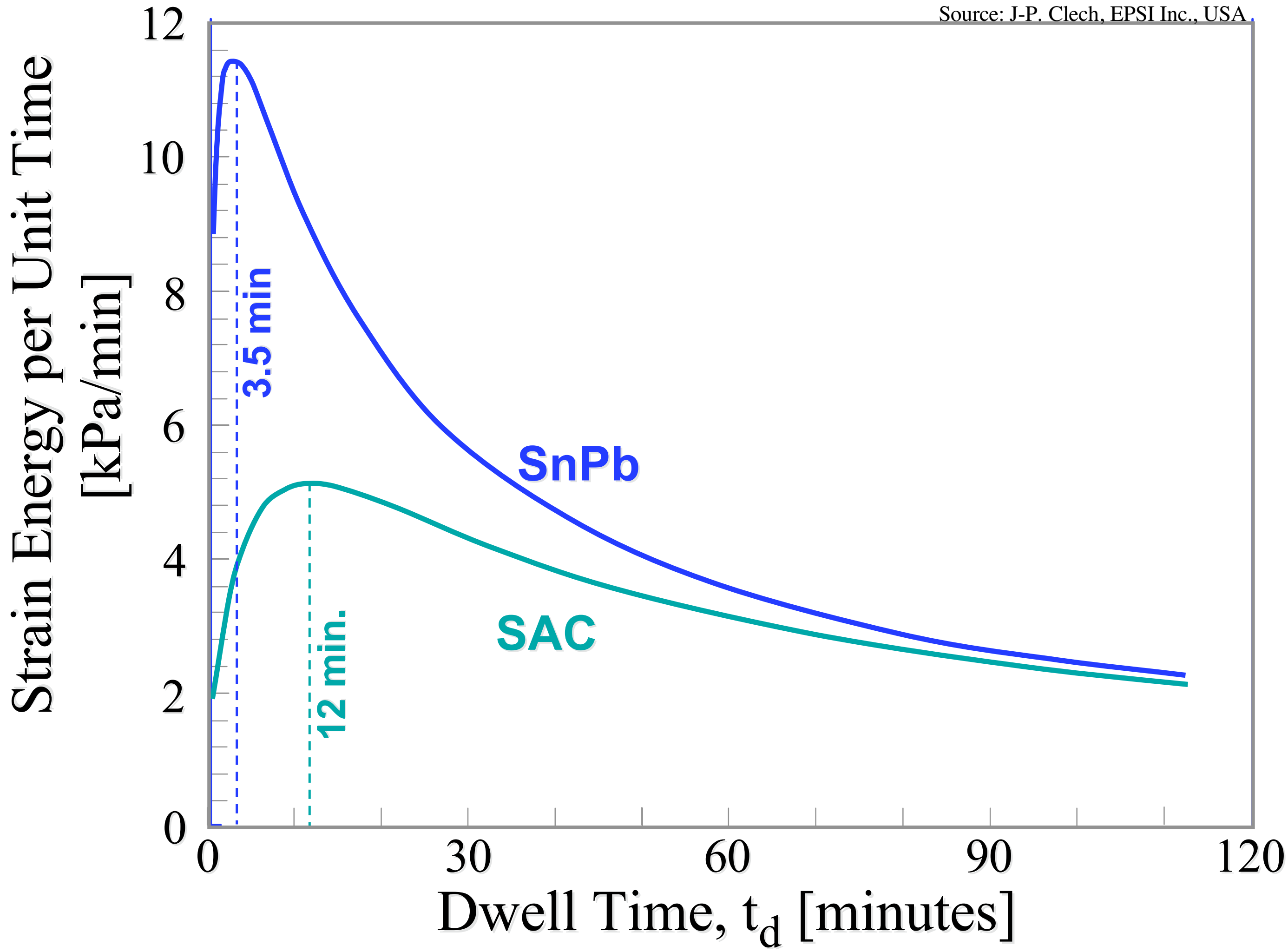
Fatigue Cycle Hysteresis Loops SAC vs. Sn/Pb Solder



Relative Life of SnPb & SAC Solder Joints in Accelerated Testing



Cyclic Fatigue Damage/ Dwell Time Dependence



Reliability Assurance Test : Solder Attachments (1)

- Accelerated Temperature Cycling
  - According to IPC-9701 "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments" & IPC-SM-785 "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments."
  - ➢ For LF-solders modify cycle by extending the dwell at low temperature extreme to 30 minutes; possibly also -20<=>+120°C to achieve results in shorter time.
  - ➢ Large data base of slow ATC required to establish acceleration factors to field reliability for LF-solders.

Reliability Assurance Test : Solder Attachments (2)

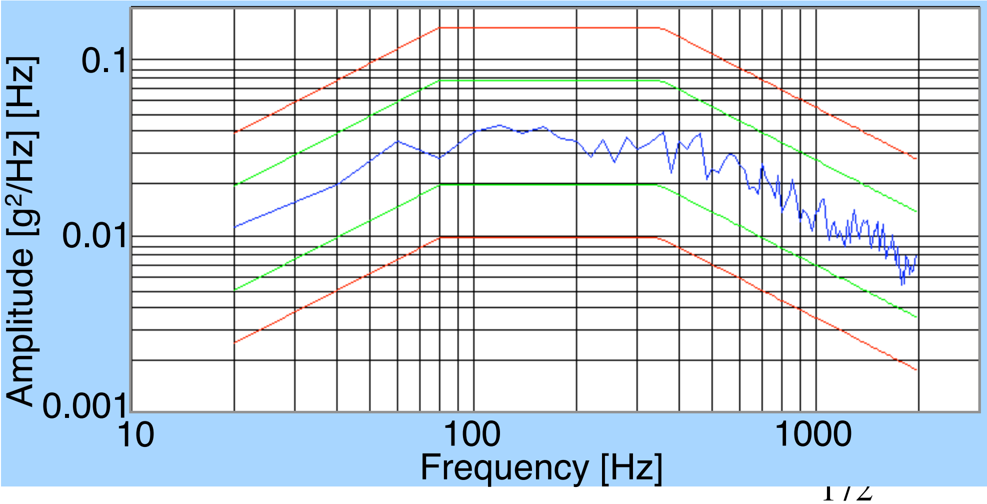
- Recommendation:
  - Use the same 'Design for Reliability'-procedure as for Sn/Pb solder joints, but use a safety factor of 2x or 3x to account for the uncertainties.
  - ➢ This recommendation is for product reliability estimates only, and does not apply to accelerated temperature cycling results.

Reliability Assurance Test : Solder Attachments (2)

- Mechanical Shock
  - No common standards exist--Bell Labs had a 3-times in 3-axes drop test from the height if a 4 drawer filing cabinet 'standard' for phones--this produces ~800 g for <5msec
  - Drop tests establish capability to withstand mechanical shock loading
  - For solder joints mechanical shock establishes robustness of the interfacial metallurgical bonds and other interfacial metallization layers

Reliability Assurance Test : Solder Attachments (3)

- Vibration
  - ➢Vibration makes a very good screening procedure that does not damage good quality solder joints.
  - – 10 minutes random vibration 20 to 2000 Hz at 0.04 g^2/Hz at PCB at room temperature; testing at -40°C increases test effectiveness--measure functionality in-situ; if not practical, do functional test after ESS with assembly mechanically exited either be some vibration or PCB bending.



Reliability Assurance Test : Printed Circuit Boards (1)

- ATC/IST/HATS Testing
  - Printed circuit board coupons are subjected to temperature cycles between some low temperature to about the glass transition temperature of the resin; coupons with the smallest PCB PTV diameter test for PTV barrel cracking whereas coupons with the largest PTV diameter test for PTV inner-layer separation
    - These tests can assure the capability of the PTH/PTV interconnect structures to withstand the increased soldering temperatures required for LF-solders

Reliability Assurance Test : PCBs (2) Accelerated Temperature Cycling/Shock

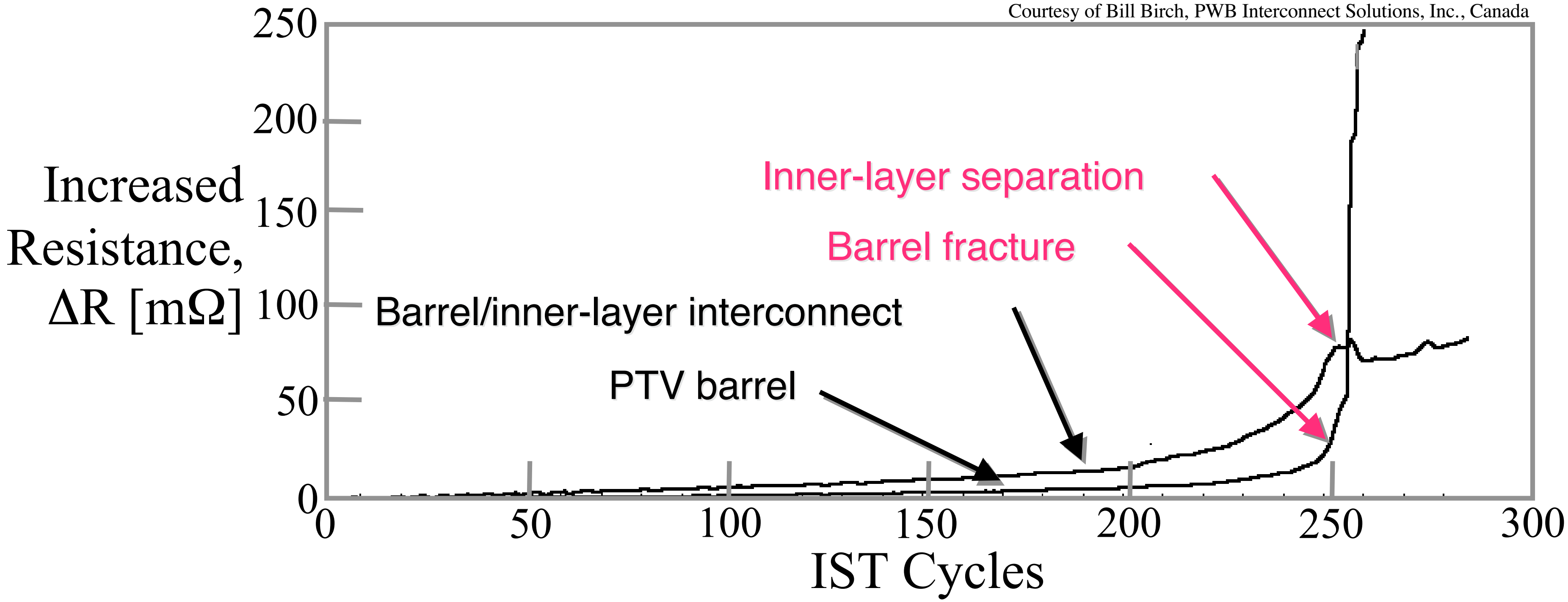
- For bare printed circuit boards, there is no difference between cycling and shock test results.

  Note: This is, of course, not true for assemblies.

- The maximum temperature should be no higher than T_g–25°C to avoid non-linear PCB resin properties confounding the test results.
- Temperature cycles used are e.g. –65<=>+125°C **[IPC-TR-579 "Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards"],** –50<=>+125°C, –40<=>+145°C, –20<=>+125°C.

Reliability Assurance Test : PCBs (3) IST(1): Damage Signatures

Courtesy of Bill Birch, PWB Interconnect Solutions, Inc., Canada



IST, internally heats PWB by resistance-heating Cu of 100 PTV/traces daisy-chains. Resistance trace for whole chain, but failure @ 1 location

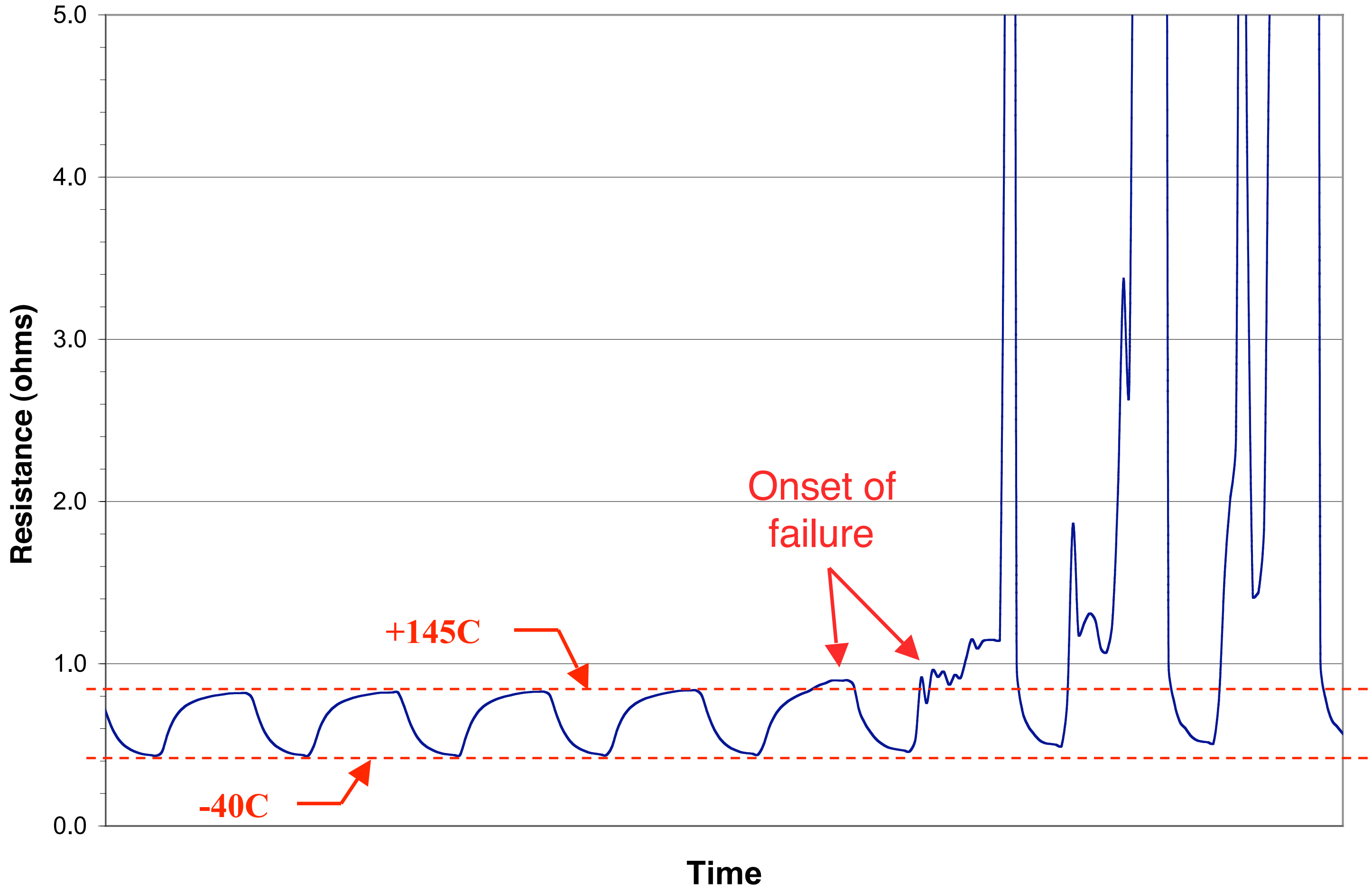
Reliability Assurance Test : PCBs (4) IST(2): Correlation

- No quantitative correlation has as yet been established between IST and either solder process temperatures or temperature cycling tests--the qualitative correlation, however, is excellent **[IPC-TR-486 "Report On Round Robin Study To Correlate Interconnect Stress Test (IST) With Thermal Stress/Microsectioning Evaluations For Detecting The Presence Of Inner-Layer Separations"]**

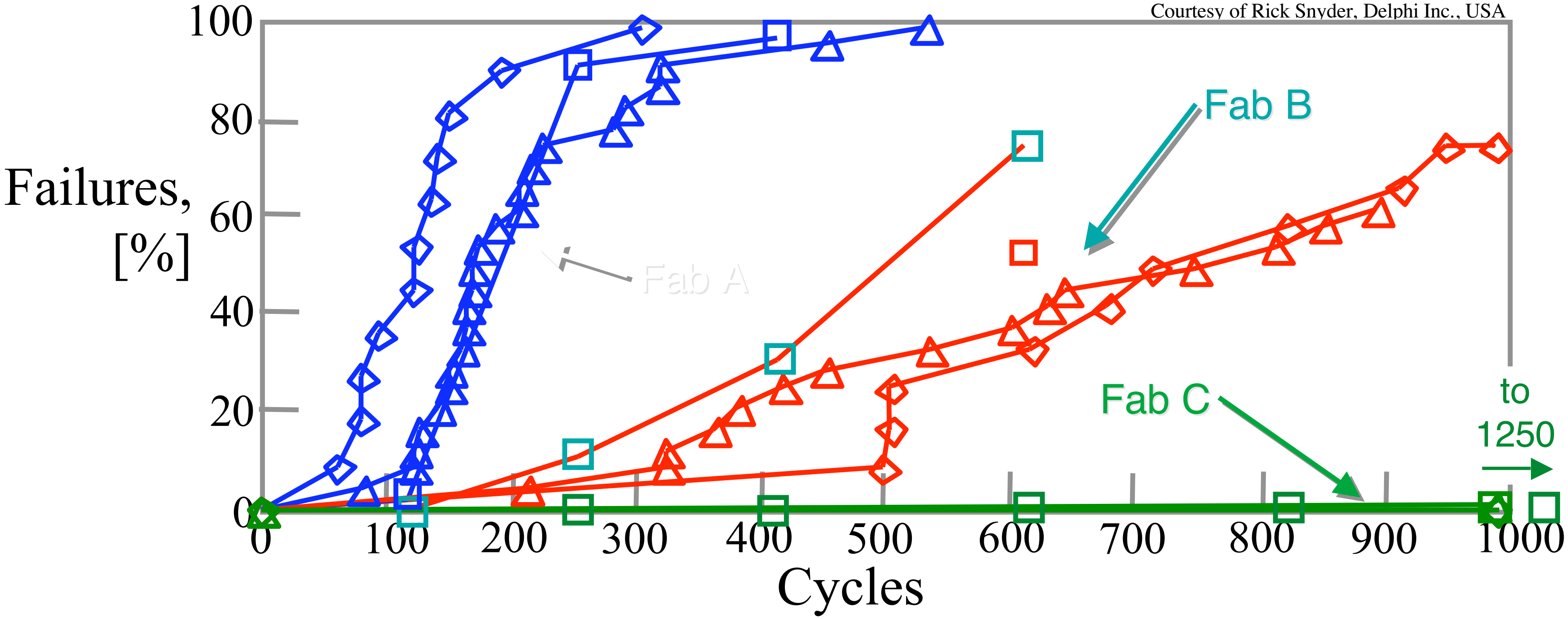
Reliability Assurance Test : PCBs (5) Highly Accelerated Thermal Shock (HATS) (1)

- HATS Testing
  - PCB coupons are subjected to temperature cycles with ranges up to –55°C⇔ +160°C, by air-to-air thermal excursions with ramp rates up 26°C/minute;
  - 36 coupons with 144 test nets can be tested simultaneously;
  - Data acquisition is by 4-wire resistance with 20 readings/second.
    - This test is capable of temperature cycle/shock testing more rapidly than such testing in a chamber because of the much smaller test volume and thermal masses involved, but is otherwise the same.

Reliability Assurance Test : PCBs (6) HATS™ Damage Signature (2)



Reliability Assurance Test : PCBs (7) Comparison: ATC, HATS & IST Results



Fabs: FR-4, T_g=170°C, 31 mil-thick PCB, 8 & 10 mil-diameter holes

- TS: -40°C⇔+145°C/60 minute cycle
- HATS: -40°C⇔+145°C/14 minute cycle
- IST: RT⇔+170°C/10 minute cycle

Reliability Assurance Test : Components

- [Simulated] Reflow Test
  - Expose components to 90%RH @ 40°C for 48 hours (do not soak in H_20, absorption rate much slower)
  - Bake-dry [vacuum bake] @105°C for 2hrs, 3 hrs, etc.; 6 hrs is known to remove ~90% of contained moisture (save to reflow solder @ 220°C/no solderability degradation)
  - Subject immediately [12 hrs @ ≥40%RH ➠ 90% re-absorption] to reflow procedure with component solder joints reaching 275°C followed by visual inspection and cross-sectioning
    - ➢ Establishes level of bake needed for component survival
    - ➢ Establishes whether component structure retains solderability

Moisture Sensitivity Levels: Floor Lives & Reflow Survival Soaks

IPC MSL Level	Floor Life (Out of Bag)	3xTest Reflow Survival After Soak Requirements (hrs @ °C/% RH)
MSL1	Unlimited@ ≤30°C/85% RH	168 @ 85/85
MSL2	1 year @ ≤30°C/60% RH	168 @ 85/85
MSL2a	4 weeks @ ≤30°C/60% RH	672 + MET @ 30/60
MSL3	1 week @ ≤30°C/60% RH	168 + MET @ 30/60
MSL4	72 hrs @ ≤30°C/60% RH	72 + MET @ 30/60
MSL5	48 hrs @ ≤30°C/60% RH	48 + MET @ 30/60
MSL5a	24 hrs @ ≤30°C/60% RH	24 + MET @ 30/60
MSL6	Mandatory Bake: Time on Label (TOL)	TOL @ 30/60

* MET = Manufacturing Exposure Time

Source: IPC/JEDEC J-STD-033B & J-STD-020D

The floor life needs to be derated at conditions >30°C/60%RH; this requires knowledge of the moisture diffusion process. Accelerated (~5x) soak conditions at 60°C/60%RH are given.

Moisture Sensitivity Levels: Floor Lives in Various Environments

IPC MSL Level	Floor Life (Out of Bag) days @ 30°C/5% RH	Floor Life (Out of Bag) days @ 30°C/60% RH	Floor Life (Out of Bag) days @ 30°C/90% RH
MSL1	Unlimited	Unlimited	365
MSL2	**Unlimited**	**365**	**365**
MSL2a	**Unlimited**	**28**	**1**
MSL3	**Unlimited**	**7**	**1**
MSL4	**Unlimited**	**3**	**1**
MSL5	**Unlimited**	**2**	**1**
MSL5a	**Unlimited**	**1**	**1**
MSL6	**Mandatory Bake: Time on Label (TOL)**		

Source: T. Sack & L. Scala, Celestica, Canada

The moisture diffusion process at various conditions results in greatly varying floor lives.

Moisture Sensitivity Levels: Required Bake/Drying Times After Excess Exposure

IPC MSL Level	Trays @ 125°C	Trays @ 90°C/≤5% RH	Tubes, Tape and Reels @ 40°C/≤5% RH
MSL1	N/A	N/A	N/A
MSL2	N/A	N/A	N/A
MSL2a	21 hrs	3 days	29 days
MSL3	27 hrs	4 days	37 days
MSL4	34 hrs	5 days	47 days
MSL5	40 hrs	6 days	57 days
MSL5a	48 hrs	8 days	79 days
MSL6	Manufacturer's recommendation		

Source: T. Sack & L. Scala, Celestica, Canada

After exposure that is too long, rebaking or drying is required.

Component Moisture Sensitivity Classification Reflow Temperatures

Package Thickness	Component Volume		
Eutectic SnPb Soldering			
	<350 mm^3	≥350 mm^3	
<2.5 mm	235°C	220°C	
≥ 2.5 mm	220°C	220°C	
Lead-Free Soldering			
	< 50 mm^3	350—2,000 mm^3	>2,000 mm^3
<1.6 mm	260°C	260°C	260°C
1.6—2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Source: IPC/JEDEC J-STD-020D

An iNEMI study has indicated that the MSL rating degrades by about one level for every 10°C increase in soldering temperature.

Relevant Documents:

- IPC-9701 “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments”
- IPC/JEDEC-9702 “Monotonic Bend Test Method for Surface Mount Solder Attachments”
- IPC-9703 “Shock Test Methods and Qualification Requirements for Surface Mount Solder Attachments”—DRAFT
- IPC-9704 “Printed Wiring Board Strain Gage Test Guideline” —DRAFT
- IPC-SM-785 “Guidelines for Accelerated Reliability Testing of Surface Mount Technology Printed Board Assemblies”
- IPC-D-279 “Design Guidelines for Reliable Surface Mount Solder Attachments”
- IPC-TR-486 “Report On Round Robin Study To Correlate Interconnect Stress Test (IST) With Thermal Stress/ Microsectioning Evaluations For Detecting The Presence Of Inner-Layer Separations”

all at http://www.ipc.org

LF-Solder Joint Reliability Info (1):

- LEADFREE [Günter Grossmann et.al., Swiss EMPA] paper: http://www.weichloeten.de/eureka-leadfree/04gg-comp-rel.pdf
- UK's National Physical Laboratory Report DEPC MPR 030 'Measuring the Reliability of Electronics Assemblies During the Transition Period to Lead-Free Soldering,' August 2005: http://tinyurl.com/t6vlt

  Also,various graphs and other information: http://www.npl.co.uk
- Dave Hillman et.al., "The Impact of Reflowing A Pb-free Solder Alloy Using A Tin/Lead Solder Alloy Reflow Profile On Solder Joint Integrity": http://www.aciusa.org/leadfree/leadfree_impact_of_reflowing_a_pbfree_solder_alloy_using_a_tin-lead_solder_alloy_reflow_profile_on_solder_joint%20_integrity.html
- Salmela, O., et.al., "Re-Calibration of Engelmaier's Model for Leadless, Lead-Free Solder Attachments," Quality and Reliability Engineering International, Vol. 23, No.4, 2007, pp. 415-29.

LF-Solder Joint Reliability Info (2):

- Osterman, M., A. Dasgupta, B. Han, "A Strain Range Based Model for Life Assessment of Pb-Free SAC Solder Interconnects", 56th Electronic Component and Technology Conference, pp. 884 - 890, May 30-June 2, 2006.
- Osterman, M., "Strain Range Approximation for Estimating Fatigue Life of Lead-Free Solder Interconnects under Temperature Cycle Loading," IPC/JEDEC Global Conference on Lead Free Reliability & Reliability Testing for RoHS Lead Free Electronics, Boston, MA, April 10-11, 2007.

Intermetallic Compounds (IMCs):

- R. J. Fields & S.R. Low, "Physical and Mechanical Properties of Intermetallic Compounds Commonly Found in Solder Joints," see: http://www.metallurgy.nist.gov/mechanical_properties/solder_paper.html

BGA Re-Balling Services

- Best Inc. (IL): http://solder.net/technical/reballing.asp
- Circuit Technology Center (MA): http://www.circuittechctr.com/
- Six Sigma (CA): http://www.sixsigmaservices.com/
- STI Electronics, Inc. (AL): http://www.stielectronicsinc.com/index.shtml
- Costs: single ceramic BGA ~$40; volume plastic simple BGAs $~15.

LF-Solders with Bismuth:

- P.L. Liu & J.K. Shang,: “Interfacial Segregation of Bismuth in Copper/Tin-Bismuth Solder Interconnect,” Scripta mater, Vol.44, 2001, pp.1019-1023, see: http://http://www.mse.uiuc.edu/faculty/Shang/Preprints/1997-2006/ScriptaBi.pdf
- P.L. Liu & J.K. Shang,: “Interfacial Embrittlement by Bismuth Segregation in Copper/Tin-Bismuth Solder Interconnect,” *J. Mater. Res.*, Vol.16, No. 6, June 2001, pp.1651-1659, see : http://www.mrs.org/s_mrs/bin.asp?CID=2274&DID=48689&DOC=FILE.PDF

LF-Solder Joint "Fragility":

- Tz-Cheng Chiu, et.al.,: "Effect of Thermal Aging on Board Level Drop Reliability of Pb-Free BGA Packages," Proc. 2004 ECTC, pp.1256-1262, see: http://www.smta.org/files/dallas_TI_voids_presentation.pdf & http://www.smta.org/files/dallas_ectc_presentation.pdf
- M. Date, et.al., "Impact Reliability of Solder Joints," Proc. 2004 ECTC, pp. 668-674.
- Peter Borgesen and Donald W. Henderson, "Fragility of Pb-Free Solder Joints," White Paper, see: http://www.pcb007.com/PDFs/WhitePaper-SACfragility1.pdf or request from borgesen@uic.com or donwhend@us.ibm.com
- P. T. Vianco, et.al., "Solid-State Intermetallic Compound Layer Growth Between Copper and 95.5Sn-3.9Ag-0.6Cu Solder," *J. Electronic Materials*, Vol. 33, No. 9, 2004.
- Z. Mei, et.al., "Kirkendall Voids at Cu/Solder Interface and Their Effects on Solder Joint Reliability," Proc. 2005 ECTC, pp.415-420.

Tin Whiskers (1):

- Data: http://nepp.nasa.gov/whisker/
- Good pictures: http://nepp.nasa.gov/whisker/experiment/exp5/
- NASA technical paper: http://nepp.nasa.gov/whisker/reference/tech_papers/brusse2002-paper-tin-whiskers-observed-on-ceramic-capacitor.pdf
- NASA slide presentation: http://nepp.nasa.gov/whisker/reference/tech_papers/brusse2002-slides-tin-whiskers-observed-on-ceramic-capacitor.pdf
- iNemi Tin Whisker Accelerated Test Program: http://www.inemi.org/cms/projects/ese/tin_whisker.html
- iNEMI Whisker Acceptance Test Requirements (July 2004): http://thor.inemi.org/webdownload/projects/ese/tin_whiskers/Tin_Whisker_Accept_paper.pdf
- D. Pinsky & E. Lambert, "Tin Whisker Risk Mitigation for High-Reliability Systems Integrators and Designers," https://www.reliabilityanalysislab.com/tl_dp_0403_TinWhiskerRiskMitigation.asp

Tin Whiskers (2):

- JEDEC Standard JESD22A121 “Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes“, May 2005.
- George Galyon, et al, “Theory Closes in on Causes of Tin Whiskers,” Global SMT & Pack., Vol. 5, No. 9, October 2005, pp. 10-14.
- iNEMI “Recommendations on Lead-Free Finishes for Components Used in High-Reliability Products” (May 2005): http://thor.inemi.org/webdownload/ projects/ese/tin_whiskers/User_Group_mitigation_May05.pdf
- iNEMI Guidelines for Subassemblies in High-Reliability Applications (June 2006): http://thor.inemi.org/webdownload/projects/ese/High-Reliability_RoHS/High_Rel_position_061206.pdf
- Robert Landman, “Tin Whiskers—A Long Term RoHS Reliability Problem,” (April 2008): http://ewh.ieee.org/r1/new_hampshire/Docs/2008-04-Tin-Whiskers.pdf
- Postings: http://www.freelists.org/archives/tinwhiskers/

Recent Information/Up-Dates:

- NIST [Carol Handwerker] Lead-Free Solder Database & NIST/NEMI Guide on Test Procedures for Developing Solder Data: http://www.boulder.nist.gov/div853/Program3_solder.htm
- Thermodynamics and phase diagram data, other properties: http://www.metallurgy.nist.gov/solder/
  http://www.boulder.nist.gov/div853/lead%20free/props01.html
- ELFNET's "Database for Properties of Lead-Free Solder Alloys”: www.univie.ac.at/cost531/downloads/Database_leadfree_v1.pdf
- Indium Corp. data: www.Pb-free.com
- Kester Corp. data: www.kester.com/en-us/leadfree/alloys.aspx
- Matte Sn vs. SnBi Plating: www.cel.com/pdf/marcomnews/japan_best.pdf

Printed Circuit Boards (PCBs):

- W. Engelmaier, “WHITE PAPER REPORT: Recommendations for PCB FAB Notes and Specifications in Printed Circuit Board Drawings for SnPb and Lead-Free Soldering Assemblies, the Qualification of PCB Shops and Activities to Assure Continued Quality,” August 2006.

Components:

- IPC/JEDEC J-STD-020C, “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices,” **July 2004**, obtain at: http://www.ipc.org

Moisture Sensitivity:

- IPC/JEDEC J-STD-033B, "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices," **July 2004**, obtain at: http://www.ipc.org
- **T. Sack & L. Scala, Celestica, Canada**
- T. Adams & S. Martell, "The Moisture Sensitivity Standard Goes Pb-Free," *Circuits Assembly*, Vol. 33, No. 9, June 2007; see: http://circuitsassembly.com/cms/cms/content/view/4342/95/
-
- F. Monette , "Handling Moisture-Sensitive Devices," *Surface Mount Technology (SMT),* Vol. 33, No. 9, March 2001; see: http://smt.pennnet.com/Articles/Article_Display.cfm?Section=Articles&Subsection=Display&ARTICLE_ID=96180

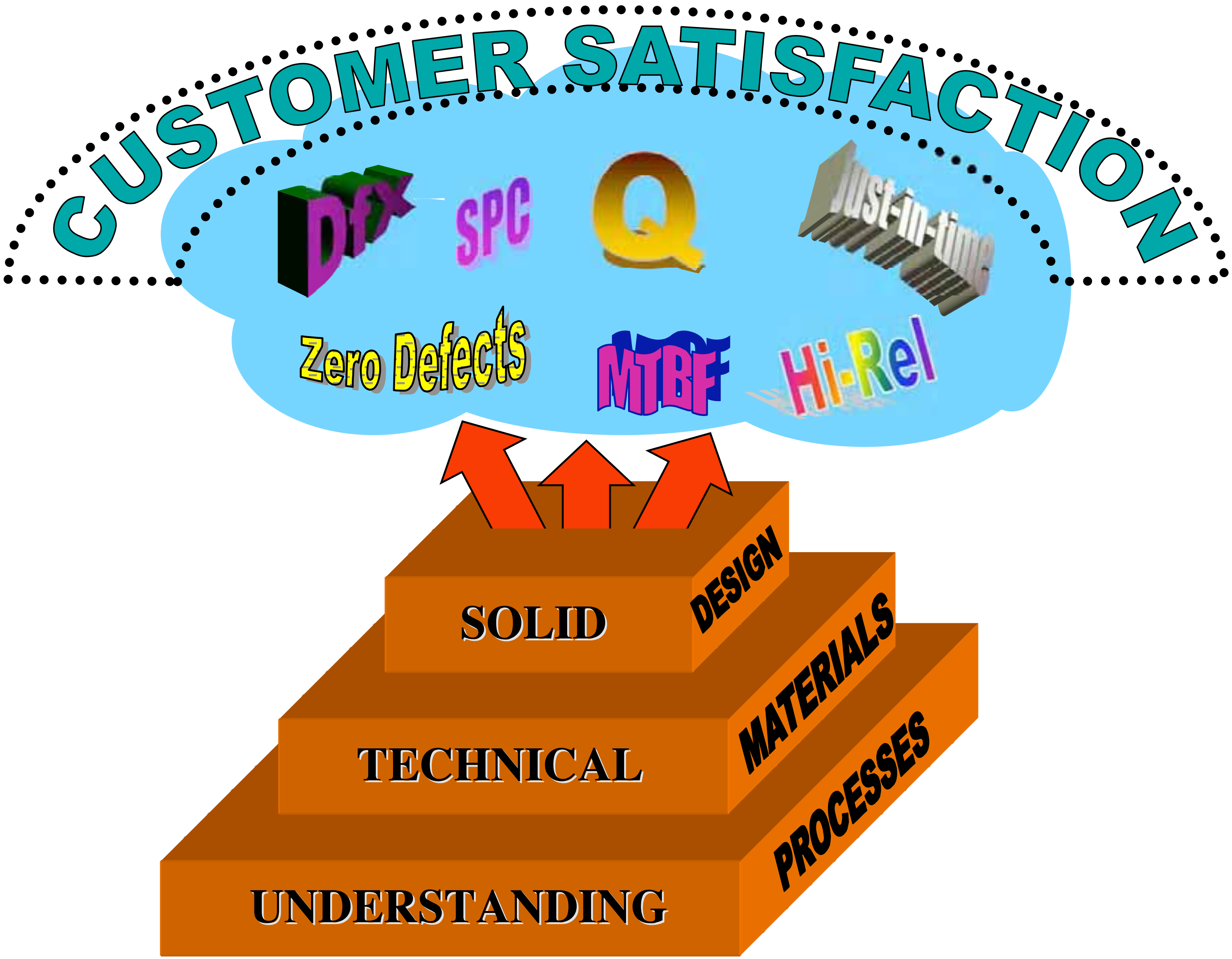
Lead-Free Solders???

- Excellent Study: http://www.cepelec.com/iso_album/leadfreehmiller.pdf
- Anti-LF-Solder Website, PLUS excellent library:

  http://www.rohsusa.com||www.rohseurope.com/||www.rohsasia.com/

No Technical Content:

- History, Calendar, Roadmap--IPC website: www.leadfree.org
- Calendar, Activities--NEMI website: http://www.nemi.org
- Good links--Fraunhofer Institut website on Soldering: http://www.weichloeten.de//click on 'bleifrei'
- Good links/search capability: http://www.tintechnology.biz
- Industry news: http://www.indium.com


CUSTOMER SATISFACTION
Dfx
SPC
Q
Just-in-time
Zero Defects
MTBF
Hi-Rel
SOLID
DESIGN
TECHNICAL
MATERIALS
UNDERSTANDING
PROCESSES

Thank you for attending!
Are there any questions?

More workshops by your lecturer:

- **Solder Joint Reliability –**
  - **Part 1: Fundamentals in Solder Joint Reliability**
  - **Part 2: Failure Mode and Root Cause Analyses (Fatigue, Brittle Fracture, ENIG)**
  - **Part 3: Acceleration Models, Accelerated Reliability Tests and Screening Procedures**
- **Interconnect Failures and Design for Reliability for Plated-Through Holes/Vias**
- **White Paper: How to Specify PCBs to Reliably Survive Lead-Free Soldering Processes**