How to estimate solder joint reliability, part 2

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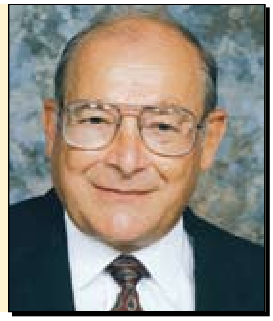

So, how does one estimate the reliability of solder attachments in an electronic system - a numerical example.

In last month's reliability column[1], I presented all the models and equations necessary to estimate the reliability of the solder attachments of the various components, individually and collectively, making up an electronic assembly.

The concepts presented in Ref. 1 underlying Design-for Reliability (DfR) procedures[2] are perhaps best illustrated by running through a numerical example that includes various components of different quantities and different loading conditions.

Numerical example

Let's run a Design for Reliability (DfR) procedure for an electronic system with a design life of 10 years with one on/off cycle per day operating in an environment where air conditioning may be down twice a year due to maintenance or failure. Thus, there are 3,630 normal operating cycles and 20 with AC failure. The acceptable failure probability at the end of the 10-year-design life is 0.5%. The system consists of five 68 I/O plastic leaded chip carriers (PLCCs), four 596 I/O plastic BGAs, thirty 1206 chip resistors (RCs), three 1825 chip capacitors (CCs), one 10 W RF power amplifier and one 144-pin surface mount connector, all surface mounted to an FR-4 PCB.

This system is designed for component variety, and not to represent a realistic system.

In *Table 1* the physical details of the various components in the system are given.

It needs to be realized that for some of the components obtaining these parameters may be far from easy. Data sheets are frequently incomplete, if not incorrect, and particularly the coefficients of thermal expansion (CTEs) may have to be measured.

Table 2 contains the thermal details for the various components in the system. To obtain these values with some accuracy requires a thermal analysis of the system.

Table 1. Physical Parameters of Components in example system.

i	Component	n	DNP (mm) (inch)	h (mm) (mils)	L (mm) (mils)	K (N/mm) (lb/in)	A (mm²) (mils²)	CTE (ppm/°C)	P (W)
1	68 I/O PLCC	5	17.1	0.076	1.52	11.7	0.39	17.0	0.5
			0.674	3.0	50.0	65	600		
2	596 I/O BGA	4	15.9	0.572	0.001	-	-	11.4	0.5
			0.625	22.2	0.025				
3	1206 RC	30	1.30	0.076	0.002	-	-	9.5	0
			0.051	3.0	0.063				
4	1825 CC	3	1.78	0.076	0.635	-	-	11.5	0
			0.070	3.0	25.0				
5	RF Amplifier	1	18.0	0.076	7.81	36.0	30.0	7.8	10
			0.709	3.0	307.5	200	46500		
6	Connector	1	30.3	0.127	0.762	16.3	0.116	12.9	0
			1.19	5.0	30	90	180		
-	PCB	-	-	-	-	-	-	16.0	-

Table 2. Thermal parameters of components in example system.

j	i	Component	P (W)	T_0 (°C)	T_S (°C)	T_C (°C)	T_{SJ} (°C)	ΔT_S (°C)	ΔT_C (°C)	ΔT_e (°C)
1	1	68 I/O PLCC	0.5	21	58	64	41.0	37	43	62.2
	2	596 I/O BGA	0.5	21	58	64	41.0	37	43	67.5
	3	1206 RC	0	21	55	55	38.0	34	34	34.0
	4	1825 CC	0	21	55	55	38.0	34	34	34.0
	5	RF Amplifier	10	21	63	75	45.0	42	54	30.6
	6	Connector	0	21	55	55	38.0	34	34	34.0
2	1	68 I/O PLCC	0.5	21	73	79	48.5	52	58	77.2
	2	596 I/O BGA	0.5	21	73	79	48.5	52	58	82.5
	3	1206 RC	0	21	70	70	45.5	49	49	49.0
	4	1825 CC	0	21	70	70	45.5	49	49	49.0
	5	RF Amplifier	10	21	78	90	52.5	57	69	45.6
	6	Connector	0	21	70	70	45.5	49	49	49.0

In Table 2 the values for $\overline{T}_{SJ}$ and DTe are calculated from *Equations 1 and 2*, respectively. The mean cyclic solder joint temperature, $\overline{T}_{SJ}$, can be calculated from

Equation 1.

$$\overline{T}_{SJ} = \frac{1}{4}\left(T_C + T_{C,0} + T_S + T_{S,0}\right)$$

where T_C, T_S = high cycle temperatures of component and substrate, respectively;

T_{C0}, T_{S0} = low cycle temperatures of component and substrate, respectively;

and ΔT_e from

Equation 2.

$$\Delta T_e = \left[\frac{CTE_C \cdot (T_C - T_{C,0}) - CTE_S \cdot (T_S - T_{S,0})}{CTE_C - CTE_S}\right]$$

Table 3. Solder joint creep-fatigue lives for components in example system [Components not meeting reliability requirements are shown in red].

			Global				Local			
j	i	Component	ΔD	N(50%) (cycles)	N(0.5%) (cycles)	N / N(x%)	ΔD	N(50%) (cycles)	N(0.5%) (cycles)	N / N(x%)
1	1	68 I/O PLCC	0.0024	114,000	22,100	0.1647	0.0032	58,700	11,400	0.3198
	2	596 I/O BGA	0.0059	15,300	2,960	1.2264	0.0000	2E+11	4E+10	0.0000
	3	1206 RC	0.0000	1E+11	2E+10	0.0000	0.0000	4E+10	8E+09	0.0000
	4	1825 CC	0.0025	108,000	20,900	0.1738	0.0266	584	113	32.1427
	5	RF Amplifier	0.0003	7E+6	1E+06	0.0027	0.0809	48	9	391.070
	6	Connector	0.0118	3,490	675	5.3786	0.0015	319,000	61,700	0.0588
2	1	68 I/O PLCC	0.0029	64,800	12,500	0.0815	0.0044	27,300	5,280	0.0038
	2	596 I/O BGA	0.0093	5,230	1,010	0.0120	0.0000	8E+10	2E+10	0.0000
	3	1206 RC	0.0000	5E+10	1E+10	0.0000	0.0000	1E+10	2E+9	0.0000
	4	1825 CC	0.0036	43,000	8,320	0.0024	0.0383	245	47	0.4221
	5	RF Amplifier	0.0000	1E+6	193,000	0.0001	0.1034	27	5	3.8305
	6	Connector	0.0246	646	125	0.1601	0.0022	126,000	24,400	0.0008

ΔT_e is to be substituted for ΔT for active components with power dissipation to account for the differences in the temperatures of the heated components and the substrate.

In *Table 3* the values for the damage terms, ΔD, the mean cyclic lives, *N*(50%), and the number of cycles to a failure probability of x=0.5%, *N*(0.5%), are given for both the global and the local thermal expansion mismatches. They are obtained using *Equations 1 through* 6 in Ref. 1.

In *Equation* 6 a Weibull slope of β=3 was used; some low acceleration tests have shown some wider distributions for leaded components than leadless components, suggesting values closer to β=4 and β=2 for leadless and leaded components, respectively.

It should be noted, that some high-acceleration tests result in tight failure distributions and large values for β; using those β-values for product reliability estimates is non-conservative *(Figure 1)*.

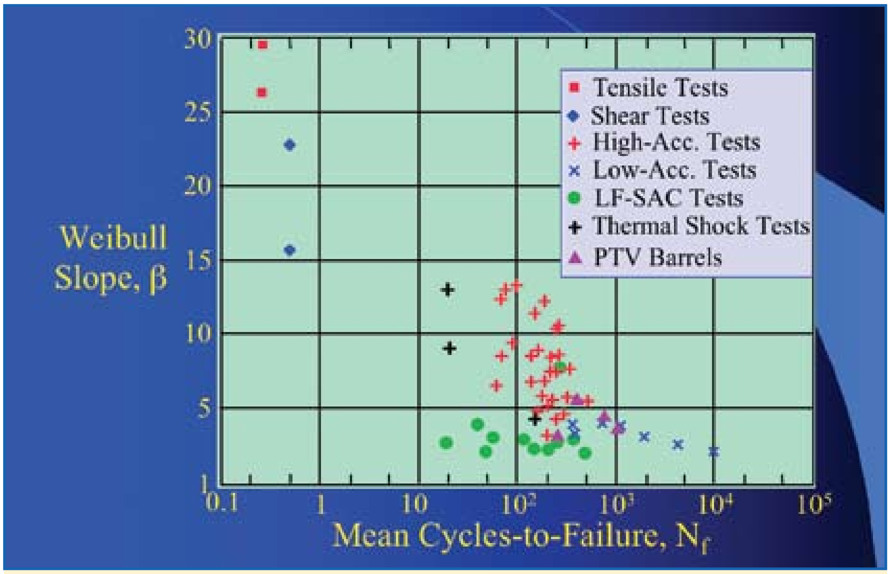

Figure 1. Weibull slope dependence on test severity.

The ratios of N, the number of expected operational cycles, and N(0.5%) are also given in *Table 3* for each individual component. Obviously, any such ratio for a given component near or exceeding unity [1.0], puts the reliability of the system in jeopardy.

The 1825 CC and the RF amplifier are a reliability threat due to the local expansion mismatch resulting from their large solder pad/attachment area dimensions. It should be noted that while local expansion mismatches will result in near-interfacial solder joint fractures, these fractures by themselves only rarely lead to functional failure because the cracks reduce the very dimensions that cause the large expansion mismatch.

In *Table 4* the failure probabilities for each component group are given both in terms of the threat to reliability from the global and local thermal expansion mismatches separately, and combined. They were calculated using *Equation* 9 in Ref.1.

Table 4. Solder joint failure probabilities for components in example system [Components not meeting reliability requirements are shown in red].

i	Component	n	Global Failure Probability	Local Failure Probability	Total Failure Probability
1	68 I/O PLCC	5	0.36%	1.35%	1.70%
2	596 I/O BGA	4	0.93%	0.00%	0.93%
3	1206 RC	30	0.00%	0.00%	0.00%
4	1825 CC	3	0.00%	100%	100%
5	RF Amplifier	1	0.00%	100%	100%
6	Connector	1	55%	0.01%	55%
	System				100%

Only the small ceramic 1206 chip resistors do not present a threat to the reliability of the example system. The 68 I/O plastic leaded chip carriers becomes a reliability liability because there are five of them.

To meet reliability requirements, five of the six components in this example 'system' need to undergo a redesign. Redesign options for the six components are:

1) 68 I/O PLCC: shorten lead foot to 30 mils;

2) 596 I/O BGA: use non-melting solder balls or options discussed in References 2 and 3;
3) 1206 RC: none needed;
4) 1825 CC: reduce width of soldering pads to 50% of component width, or comb-pattern soldering pads;
5) RF amplifier: comb-pattern amplifier leads and soldering pads in orthogonal directions;
6) Connector: use connector body material with CTE tailored closer to the PCB CTE and/or increase lead compliancy.

The above example is illustrative of the root cause of the rash of recent failures in consumer electronics[5-8] and laptop computers[9-11]. *Figure 2* shows a 'unique' temporary repair method.

It appears that with the increasing functionality, improved battery capabilities, and shrinking product size, the operating temperatures have risen sufficiently, and the serendipity-approach previously taken with consumer products is no longer adequate to assure reliability.

Figure 2. 'Unique' temporary repair method to press solder joint fracture surfaces together - yes, this is a C-clamp[11].

References

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Werner Engelmaier will be giving some of his solder joint reliability and PCB reliability workshops at the JEDEC/IPC Global Conferences on Lead Free Reliability and Reliability Testing for RoHS Lead Free Electronics in Austin, TX, December 3-5, 2007; for details of the workshop go to www.engelmaier.com; for more information about the workshop in Austin contact www.ipc.org

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